# An Active-Balun-Based Single-In Differential-Out K-Band LNA with High Gain and Low DC Power Consumption

**To-Po Wang, Zong-Wei Li**

***Abstract*—This paper presents an active-balun-based single-in differential-out K-band low-noise amplifier (LNA). The proposed active balun adopts separated dc-current paths for lowering the supply voltage and dc power, leading to the active balun with 0.6-V low supply voltage and 1.36-mW low dc power. Based on the proposed circuit architecture, the K-band LNA has been designed in 0.18-□m RF CMOS process. Simulated results confirm the LNA combining the proposed low-voltage low-power active balun can effectively achieve superior overall performance in terms of gain and dc power consumption. The presented LNA combing the proposed active balun exhibits a high gain of 22.1 dB and a low dc power of 5.87 mW at 24 GHz.**

***Index Terms*—active balun, low noise amplifier (LNA), single-in differential-out.**

## I. INTRODUCTION

Due to the high-data-rate wireless transmission in K band, the low noise amplifiers with operation frequencies around 24 GHz were reported [1]-[9]. In [1], a 24-GHz transformer-based single-in differential-out CMOS low-noise amplifier was presented. A trifilar transformer was utilized between the first and second stages of the LNA. It exhibits a differential gain of 14.7 dB, a noise figure of 4.3 dB, and a power consumption of 20.2 mW. To achieve a low-power low-noise amplifier in K-band, a transformer feedback was utilized [7]. By adopting a current-reused technique between amplifier's two stages, the 0.18-μm LNA exhibited 10.1 dB maximum power gain at 1.8-V supply voltage, and the dc power consumption is 7.2 mW. The noise figure is 4.3 dB.

In order to reduce the supply voltage and dc power dissipation of a K-band CMOS LNA, dc current paths were split [8]. This technology resulted in a reduction of a half of the supply voltage and minimized dc power. The 0.18-μm CMOS LNA achieved a peak gain of 13.2 dB at 20.5 GHz, a supply voltage of 0.6 V, and a dc power consumption of 7.1 mW. In [9], the quality factor improvement of the micromachined suspended inductors and their usage in a fully integrated 0.18-μm CMOS microwave amplifier was presented. At a supply voltage of 0.85 V, the peak gain of the microwave amplifier was significantly increased from 12.3 dB to 13.7 dB because of the high *Q*-factor suspended inductors.

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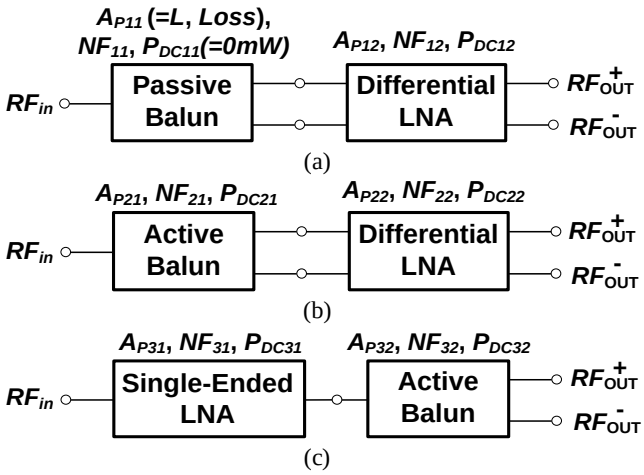


Fig. 1. Functional blocks of single-in differential-out amplifier circuits. (a) passive balun cascaded with differential LNA, (b) active balun cascaded with differential LNA, (c) single-ended LNA cascaded with active balun.

Moreover, the noise figure of the 24-GHz amplifier is improved from 5.8 dB to 5.0 dB.

## II. PROPOSED SINGLE-IN DIFFERENTIAL-OUT LNA

Fig. 1 shows the functional blocks of single-in differential-out amplifier circuits. These amplifier circuits shown in Fig. 1(a), Fig. 1(b), and Fig. 1(c) consist of two stages. For the amplifier in Fig. 1(a), the overall small signal gain ($G_1$) can be written as

$$G_1 = A_{P11} + A_{P12} = -L_{11} + A_{P12}\ (dB) \qquad (1)$$

where $A_{P11}$ and $A_{P12}$ are the gain of the first and second stage, respectively. The $A_{P11}$ can be represented by the loss ($-L_{11}$) of the passive balun. Moreover, the noise figure ($NF_1$) of the amplifier in Fig. 1(a) can be driven as

$$NF_1 = NF_{11} + \frac{NF_{12} - 1}{A_{P11}} = L_{11} + L_{11}\left(NF_{12} - 1\right)(dB) \qquad (2)$$

where $NF_{11}$ and $NF_{12}$ are the noise figure of the first stage and second stage, respectively. The $NF_{11}$ can be represented by the loss ($L_{11}$) of the passive balun in the first stage. From (2), it is observed that the noise figure for the amplifier in Fig. 1(a) is increased due to the passive balun. Furthermore, the overall dc power dissipation ($P_{DC1}$) of the amplifier circuit in Fig. 1(a) is



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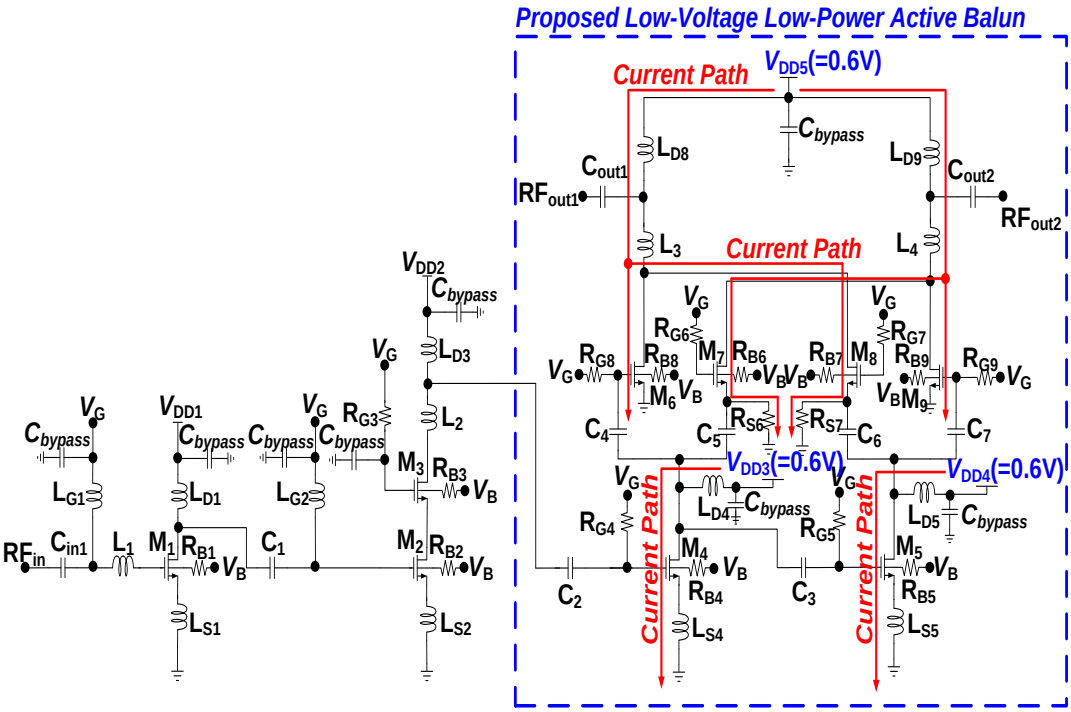


Fig. 2. Schematic of the LNA with the proposed low-voltage low-power active balun.

$$P_{DC1} = P_{DC11} + P_{DC12} = 0 + P_{DC12} = P_{DC12}\ (mW) \quad (3)$$

where $P_{DC11}$ and $P_{DC12}$ are the dc power dissipation of the first stage and second stage, respectively.

In order to improve the overall gain and noise figure of the amplifier circuit in Fig. 1(a), the passive balun can be replaced by an active balun, as shown in Fig. 1(b). Therefore, the overall gain of the amplifier is

$$G_2 = A_{P21} + A_{P22}\ (dB). \quad (4)$$

Assume the differential LNAs in Fig. 1(a) and Fig. 1(b) are identical. Compare (1) and (4), it is indicated that the overall signal gain of the single-in differential-out amplifier can be improved by

$$G_2 - G_1 = A_{P21} + L_{11}\ (dB). \quad (5)$$

In addition, the noise figure of the amplifier circuit in Fig. 1(b) is

$$NF_2 = NF_{21} + \frac{NF_{22} - 1}{A_{P21}}\ (dB) \quad (6)$$

Compare (2) and (6), it is observed that the circuit in Fig. 1(b) can achieve lower noise figure ($NF_2$) than that of the circuit in Fig. 1(a) due to the positive gain stage (i.e. active balun). The overall noise figure of the single-in differential-out amplifier can be improved by

$$NF_1 - NF_2 = (L_{11} - NF_{21}) + \left(L_{11} - \frac{1}{A_{P21}}\right)(NF_{22} - 1)\ (dB). \quad (7)$$

However, the total dc power consumption of the amplifier circuit in Fig. 1(b) is higher than that of the amplifier circuit in Fig. 1(a) due to the active balun.

To reduce the total dc power consumption, the differential LNA in Fig. 1(b) can be replaced by a single-ended LNA, as shown in Fig. 1(c). Assume the active baluns in Fig. 1(b) and Fig. 1(c) are identical. The reduced dc power consumption can be formulated as

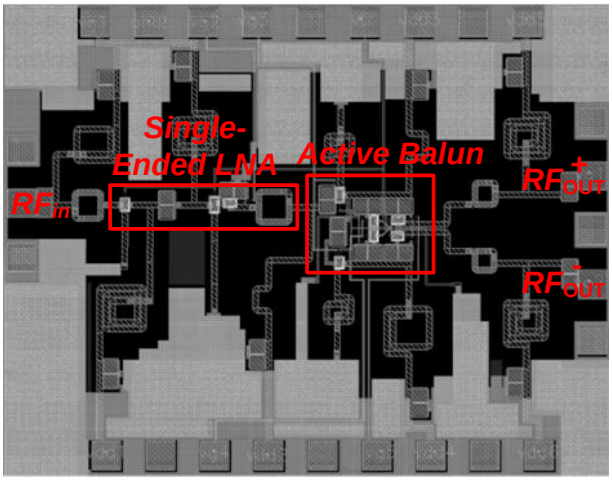


Fig. 3. Chip layout of the proposed single-in differential-out LNA with the chip size of 0.865 × 1.12 mm$^2$.

$$P_{DC22} - P_{DC31} \approx \frac{P_{DC22}}{2}\ (mW). \quad (8)$$

Fig. 2 shows the circuit schematic of the proposed single-in differential-out LNA. This LNA is designed in 0.18-μm RF CMOS process, which has six metal layers and one poly layer. To deliver high signal gain with low dc power consumption, a single-ended LNA cascaded with an active balun is adopted in this work. Moreover, the current paths of the cascode stages for the active balun in Fig. 2 are separated, leading to the reduced supply voltages ($V_{DD3}$=$V_{DD4}$=$V_{DD5}$=0.6 V). This can provide design flexibilities for different dc-current requirements of MOSFETs ($M_4$-$M_9$).

## III. SIMULATION RESULTS

The proposed single-in differential-out LNA has been designed in 0.18-μm RF CMOS process. Fig. 3 shows the chip layout of the proposed LNA. The chip size is 0.865 x 1.12 mm$^2$ including the testing pads. The supply voltages of



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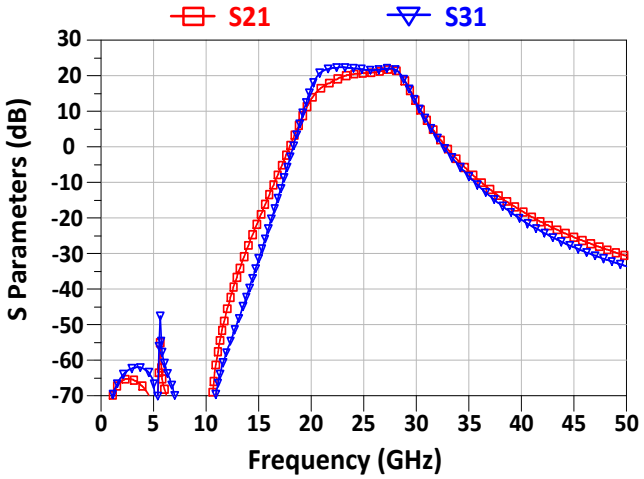
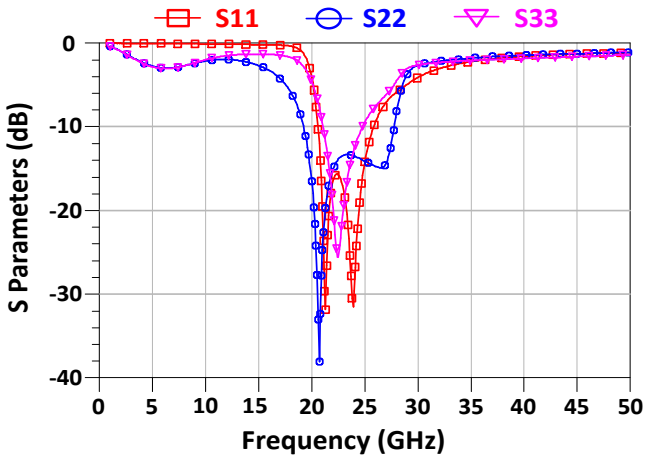



(a)



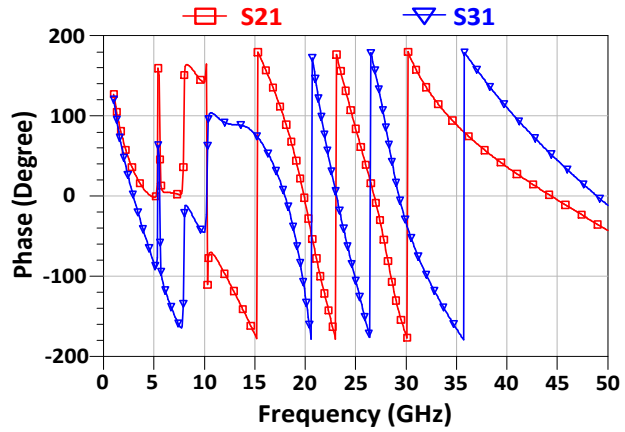

(b)

Fig. 4. (a) Simulated S parameters (gain: S21 and S31) of the proposed LNA. (b) Simulated S parameters (input return loss: S11, S22, and S33).

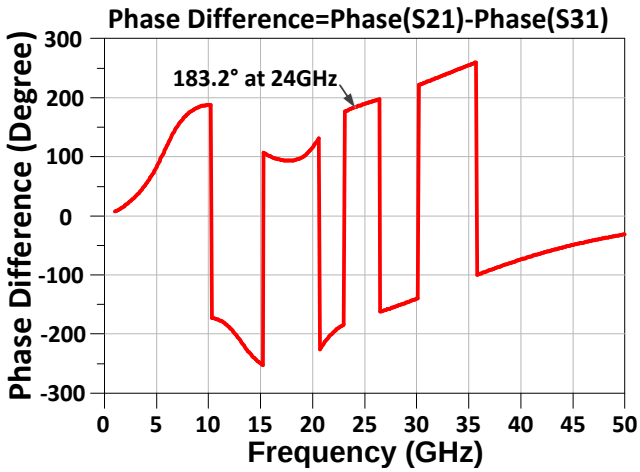
this LNA are $V_{DD1}$=$V_{DD2}$=1.2 V and $V_{DD3}$=$V_{DD4}$=$V_{DD5}$=0.6 V. The total dc power consumption of the proposed LNA is only 5.87 mW. The simulation is performed by using circuit simulator Agilent's Advanced Design System (ADS) software.

Fig. 4(a) shows the simulated S parameters of the proposed single-in differential-out LNA. From this figure, it is indicated that the peak gains of S21 and S31 are 22 dB. Fig. 4(b) shows the simulated input return loss of the proposed LNA. From this figure, it is observed that the S11, S22, and S33 are below -10 dB around 24 GHz, leading to the well matched circuits. Moreover, the simulated phases of S21 and S31 are illustrated in Fig. 5(a). It is known that the required phase can be achieved around 24 GHz. To gain more insight to the reality, the simulated phase difference between S21and S31 is depicted in Fig. 5(b). A phase difference of 183.2° at 24 GHz is exhibited. In addition, the simulated noise figure of the proposed single-in differential-out LNA is shown in Fig. 6. From this figure, it is observed that the noise figure at 24 GHz is 4.5 dB.

Table I summarizes the performance of this work and compared with the recently published 24-GHz 0.13-µm and 0.18-µm CMOS LNAs. It is indicated that the proposed single-in differential-out LNA exhibits high gain of 22.1 dB, low dc power consumption of 5.87 mW, and comparable noise figure of 4.5 dB.




(a)




(b)

Fig. 5. (a) Simulated phase of the proposed single-in differential-out LNA. (b) Simulated phase difference of the proposed single-in differential-out LNA.

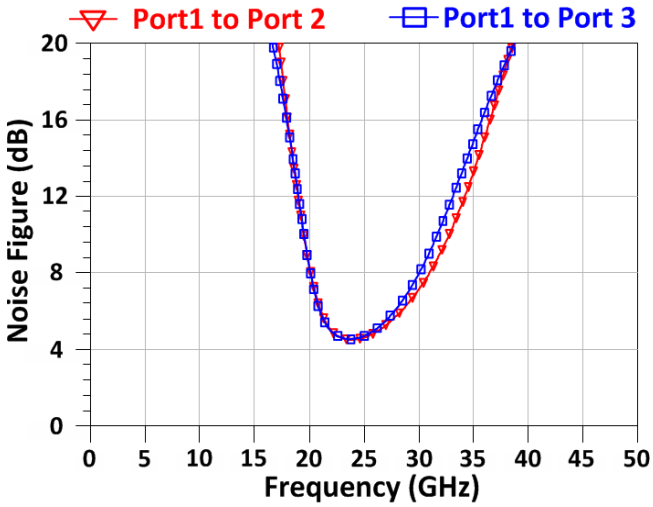



Fig. 6. Simulated noise figure of the proposed single-in differential-out LNA.

## IV. CONCLUSION

A 24-GHz single-in differential-out LNA using dc-current-path separated active balun for low dc power and high gain is proposed. By cascading the single-ended amplifier and the low-voltage low-power active balun, the overall small-signal gain can be significantly increased. Moreover, the total dc power



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Table I. Performance summary and comparison to the recently published 24-GHz LNAs

| Process | Peak Gain Freq. (GHz) | Gain (dB) | NF (dB) | $P_{DC}$ (mW) | $V_{DD}$ (V) | Chip Size ($mm^2$) | Topology | Ref. |
|---|---|---|---|---|---|---|---|---|
| 0.13-µm CMOS | 24 | 14.7 | 4.3 | 20.2 | 1.5 @1st stage 1.0 @ 2st stage | 0.828 (excluding pads) | Single-In Differential-Out Cascode+CS Transformer Based | [1] RFIC'09 |
| 0.13-µm CMOS | 23.6 | 9.2 | 3.7 | 2.78 | 1.0 | 0.448 | 2-stage CS | [2] MWCL'10 |
| 0.18-µm CMOS | 25.7 | 8.9 | 6.93 | 54 | 1.8 | 0.735 | 3-Stage CS | [3] MWCL'04 |
| 0.18-µm CMOS | 23.7 | 12.86 | 5.6 | 54 | 1.8 | 0.735 | 3-Stage CS | [3] MWCL'04 |
| 0.18-µm CMOS | 24 | 13.1 | 3.9 | 14 | 1.0 | 0.342 | 2-Stage CS | [4] MWCL'05 |
| 0.18-µm CMOS | 24 | 12.8 | 3.3 | 8 | 1.0 | 0.553 | 2-Stage CS | [5] RFIC'08 |
| 0.18-µm CMOS | 24 | 10.2 | 5.9 | 27 | 1.8 | 0.392 (excluding pads) | CS+Cascode | [6] RWS'09 |
| 0.18-µm CMOS | 22 | 10.1 | 4.3 | 7.2 | 1.8 | 0.128 (core size) | 1-stage CS &Transformer | [7] MWCL'09 |
| 0.18-µm CMOS | 20.5 | 13.2 | 4.1 | 7.1 | 0.6 | 1.36 | CS+Cascode & Split DC-Current-Path | [8] MWCL'10 |
| 0.18-µm CMOS | 22.2 | 9.0 | 7.2 | 8.04 | 0.6 | 1.053 | CS+Cascode & Split DC-Current-Path | [9] TED'13 |
| 0.18-µm CMOS | 23.1 | 10.33 | 6.0 | 7.86 | 0.6 | 1.053 | CS+Cascode & Split DC-Current-Path & MEMS inductor | [9] TED'13 |
| 0.18-µm CMOS | 23.0 | 12.3 | 5.8 | 18.4 | 0.85 | 1.053 | CS+Cascode & Split DC-Current-Path | [9] TED'13 |
| 0.18-µm CMOS | 23.5 | 13.7 | 5.0 | 17.0 | 0.85 | 1.053 | CS+Cascode & Split DC-Current-Path & MEMS inductor | [9] TED'13 |
| **0.18-µm CMOS** | **24** | **22.1** | **4.5** | **5.87** | **1.2 @1st-2nd stages 0.6 @ 3rd stage** | **0.969** | **Single-In Differential-Out CS+Cascode & Active Balun** | **This Work (Simu.)** |

dissipation of the single-ended LNA and active balun can be minimized. The proposed techniques have been designed and verified by using 0.18-µm RF CMOS process. According to the simulation results, the gain and dc power of the proposed single-in differential-out LNA are superior to that of recently published 24-GHz 0.13-µm and 0.18-µm CMOS LNAs [1]-[9].

## ACKNOWLEDGMENT

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