A 0.4-V 2.4-mW 13.4-dB Ultra-Wideband Low-Noise Amplifier with Embedded Transformers

To-Po Wang, Jing- Shiang Huang, You-Fu Lu

Abstract— A low-voltage low-power high-gain ultra-wideband (UWB) low-noise amplifier (LNA) with embedded transformers is proposed in this paper. The LNA consists of two stages, and each stage is a cascode topology. The transformer is inserted between the cascode stages for interstage impedance matching to achieve high gain. Furthermore, transformers are adopted to the common-source MOSFETs for impedance matching and supplying gate voltages. According to the proposed circuit topology, the UWB LNA has been designed in 0.18-μm CMOS process. Simulated results confirm the UWB LNA combining the transformers can effectively achieve high gain of 13.4 dB, low noise figure of 3.37 dB, low LNA supply voltage of 0.4 V, and total dc power consumption of 2.4 mW.

Index Terms—interference rejection, low-noise amplifier (LNA), noise figure, notch filter.

I. INTRODUCTION

Requirements of high-speed wireless transmission and wideband capacity are urgent. Moreover, researches for radio-frequency integrated circuits (RFICs) are increased to pursue high performance. For UWB circuits, LNA is typical the first stage for lowering a receiver's noise figure and amplify the weak message signals [1]-[10]. In [1], a 3.1-10.6-GHz UWB LNA using broadband noise-canceling technique is presented. The noise from the matching device can be suppressed, and the noise from other devices is minimized due to the noise-canceling topology. These result in a 0.18-µm CMOS LNA with 9.7-dB peak gain, 4.5-dB minimum noise figure, 1.8-V supply voltage, and 20-mW dc power consumption.

To provide wideband input matching with low noise figure (NF), a resistive shunt feedback topology is used [2]. The presented LNA is with two stages for high gain. The first stage is the cascode structure with feedback resistor connected between the drain and gate terminals of a common-source MOSFET. The later stage is a common-source stage with a resistive feedback. Based on the topology, The UWB LNA in [2] exhibits the maximum gain of 15 dB, minimum noise figure of 4.0 dB, supply voltage of 1.8 V, and dc power consumption of 21.5 mW. In [3], a CMOS UWB LNA with dual-*RLC*-branch wideband input matching network is presented. The dual-*RLC* branches is composed of a resistive shunt-shunt feedback and a parallel *LC* load. According to this topology, the UWB

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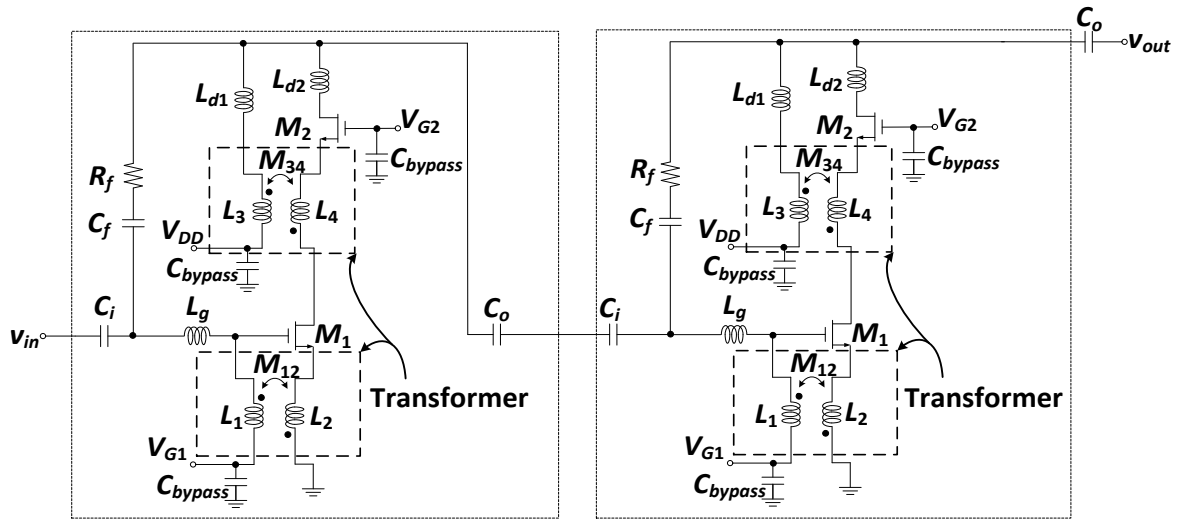
LNA achieves the maximum gain of 12.9 dB, minimum noise figure of 3.7 dB, supply voltage of 1.8 V, and dc power consumption of 10.34 mW.

To lock the in-band interferences, a UWB LNA with tunable interference rejection is presented [7]. The UWB LNA embeds a tunable active notch filter to achieve an improved interference rejection. The LNA exhibits the maximum power gain of 13.2 dB and the lowest noise figure of 4.5 dB. In addition, the interference rejection is 8.2 dB and the dc power dissipation is 23 mW from 1.8-V supply voltage. In [9], a parallel-to-series resonant matching network between common-gate and common-source stages is adopted to CMOS wideband LNAs. The LNA consists of two stages, the first stage is the common-gate stage, and the second stage is the common-source stage. Due to the interstage matching technology, the wideband LNA achieves the 12.7-dB maximum gain, 2.5-dB minimum noise figure, 0.7-V supply voltage of the first stage, 1.5-V supply voltage at second stage, and 13.4-mW dc power consumption.

To achieve a flat small signal gain covering a wide bandwidth, the *RC* shunt-shunt feedback is used [10]. In addition, the output terminal is with a parallel *RLC* load. Based on the techniques, the 0.18-µm CMOS UWB LNA exhibits the maximum gain of 13.33 dB, minimum noise figure of 2.68 dB, supply voltage of 1.8 V, and dc power consumption of 11.8 mW.

In this work, a wideband CMOS LNA with embedded transformers is presented. The transformers are used for interstage matching between the common-source and common-gate MOSFETs of the cascode topology. Therefore, the proposed UWB LNA using the proposed techniques achieves the superior performance in terms of   supply voltage, dc power consumption, gain, and noise figure.

II. PROPOSED WIDEBAND LNA

Fig. 1 shows the schematic of the proposed 3.1-10.6-GHz UWB LNA with embedded transformers. To exhibit low-voltage and high gain, two cascode stages are cascaded. Moreover, the transformers are inserted between the cascode stages for interstage impedance matching to achieve high gain. Furthermore, transformers are adopt to the common-source MOSFETs for impedance matching and supplying gate voltages. Figs. 2 and 3 depict the type-I and type-II transformers, respectively. For the type-I transformer, the ports 1 and 3 are closed located, and the ports 2 and 4 are placed in opposite direction. In addition, the type-II transformer is with more symmetrical topology than the type-I transformer. The ports (1, 4) and ports (2, 3) are arranged in the opposite directions. Fig. 4 shows the simulated inductance of the proposed type-I and type-II transformers. From this figure, it is observed that the inductance of L_1, L_2, L_3, and L_4 at 7 GHz are 2.62 nH, 0.33

Fig. 1. Schematic of the proposed UWB LNA with embedded transformers.

Fig. 2. Proposed type-I transformer.

Fig. 3. Proposed type-II transformer.

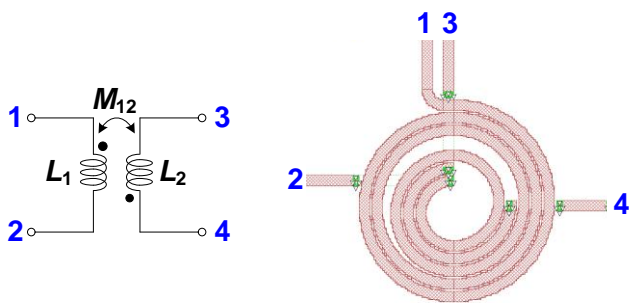Fig. 4. Simulated inductance of the proposed type-I and type-II transformers.
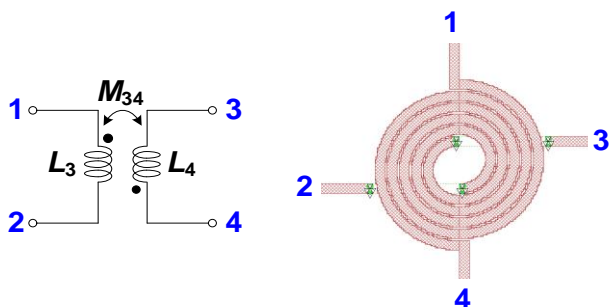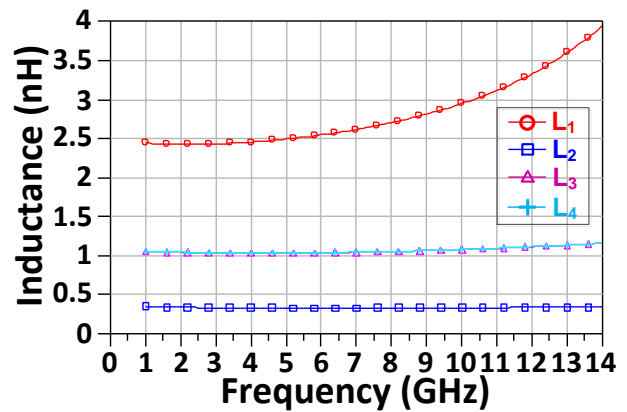

Fig. 5. Simulated quality factor of the proposed type-I and type-II transformers.

nH, 1.04 nH, and 1.04 nH, respectively. Fig. 5 depicts the simulated quality factor of the proposed type-I and type-II transformers. From this figure, it is indicated that the quality factor of L_1, L_2, L_3, and L_4 at 7 GHz are 13.4, 7.4, 11.4, and 11.4, respectively.

III. SIMULATION RESULTS

Fig. 6 shows the chip layout of the proposed UWB LNA with embedded transformers. The chip size is 1.15 x 1.13 mm^2 including the testing pads. The proposed low-voltage low-noise high-gain UWB LNA with embedded transformers has been designed in 0.18-μm RF CMOS process. The simulation is performed by using circuit simulator Agilent's Advanced Design System (ADS) software. In addition, the inductors, capacitors, and interconnections are considered by adopting full-wave electronic-magnetic (EM) simulation tools, Sonnet and HFSS.
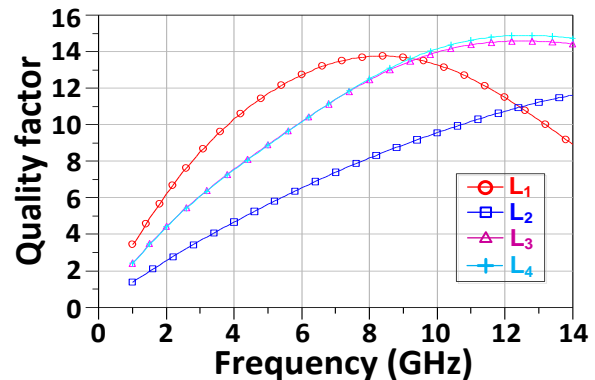
The supply voltage of this proposed UWB LNA is 0.4 V. The total dc power consumption of the UWB LNA is 2.4 mW.

Fig. 7 shows the simulated S parameters of the proposed UWB LNA. From this figure, it is observed that the maximum gain of S_{21} is 13.4 dB. Moreover, the input/output reflection coefficients (S_{11} and S_{22}) are below -10 dB for 3.1-10.6-GHz UWB bandwidth, performing the well matched input/output circuits. Fig. 8 shows the simulated noise figure of the proposed 3.1-10.6-GHz UWB LNA. It is indicated that the minimum noise figure is 3.37 dB at 7.5 GHz. To consider the linearity of the UWB LNA, the simulated input-referred third-order intercept point (IIP$_3$) of
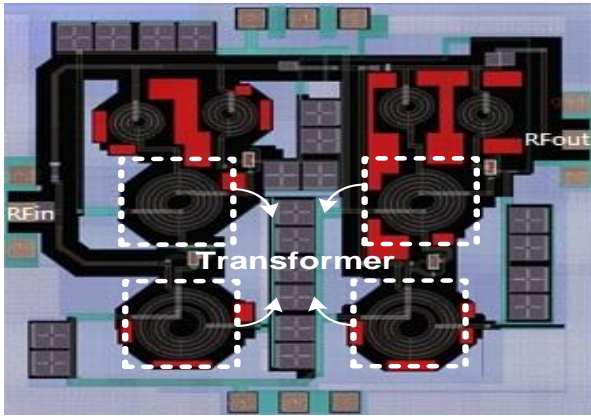
Fig. 6. Chip layout of the proposed UWB LNA with embedded transformers (the overall chip size is 1.15×1.13 mm^2).

the proposed UWB LNA is shown in Fig. 9. The two-tone test is carried out, and the frequency spacing is 1 MHz. It is indicated that the IIP$_3$ for the proposed UWB LNA is -13 dBm. Table I summarizes the performance of the presented UWB LNA and compared to the recently published 0.18-μm CMOS UWB LNAs. From this table, it is observed that the proposed UWB LNA exhibits good performance in terms of supply voltage, dc power consumption, gain, and noise figure.

IV. CONCLUSION

The 3.1-10.6-GHz UWB LNA with embedded transformers is proposed in this paper. Based on the proposed type-I and type-II transformers, the UWB LNA can deliver high gain of 13.4 dB, low noise figure of 3.37 dB, low LNA supply voltage of 0.4 V, and total dc power consumption of 2.4 mW. Compared to the previous published 0.18-μm CMOS UWB LNA, the proposed circuit topology in this work exhibits superior performance in terms of supply voltage, dc power consumption, gain, and noise figure.

ACKNOWLEDGMENT
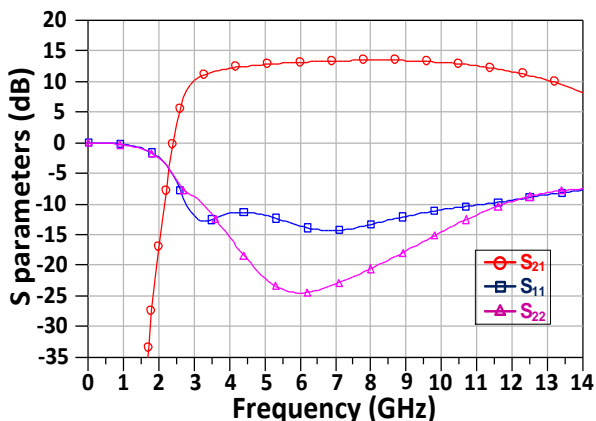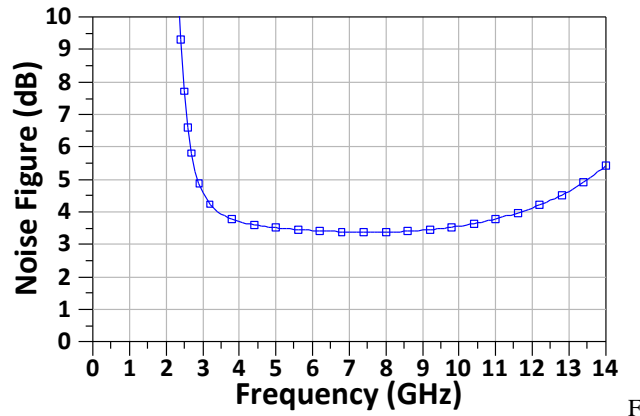
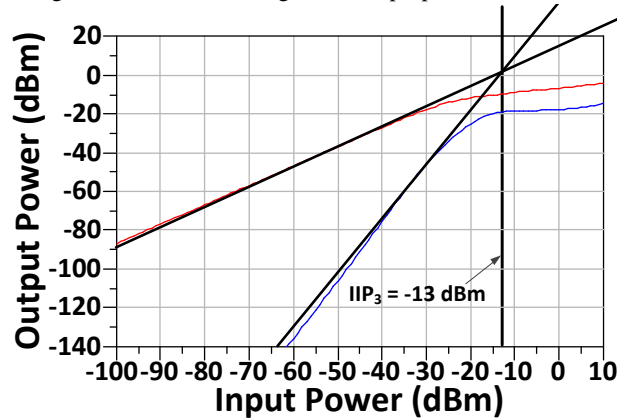Fig. 8. Simulated noise figure of the proposed UWB LNA.

Fig. 9. Simulated input-referred third-order intercept point (IIP3) of the proposed UWB LNA.

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Fig. 7. Simulated S parameters of the proposed UWB LNA.

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Table I. Performance summary and comparison to the recently published 0.18-μm CMOS UWB LNAs

Process	3-dB BW (GHz)	Max Gain (dB)	S11 (dB)	S22 (dB)	Min. NF (dB)	NF (dB) (3.1–10.6GHz)	Supply Voltage (V)	DC Power (mW)	Ref.
0.18-μm CMOS	10.7 (1.2–11.9)	9.7	< -11	< -10	4.5	4.5–5.1	1.8	20	[1] JSSC'07
0.18-μm CMOS	7.4 (3–10.6)	15	< -7	< -8	4.0	4.0–4.4	1.8	21.5	[2] SiRF'10
0.18-μm CMOS	10.2 (1.5–11.7)	12.9	< -8.6	< -10	3.7	3.74–4.74	1.8	10.34	[3] TMTT'10
0.18-μm CMOS	7.5 (3.1–10.6)	14	< -11	n.a.	4.5	~4.5	1.8	21	[4] TMTT'10
0.18-μm CMOS	7.5 (3.1–10.6)	12	< -13.5	< -10 .1	5.27	5.27-7	1.5	4.5	[5] TMTT'10
0.18-μm CMOS	10.5 (0.5–11)	10.2	<-9	<-6	3.9	3.9–4.5	n.a.	14.4	[6] MWCL'10
0.18-μm CMOS	7.5 (3.1–10.6)	13.2	< -10	n.a.	4.5	4.5–6.2	1.8	23	[7] MWCL'10
0.18-μm CMOS	8 (2.0–10.0)	20	<-12	n.a.	2.4	2.4-3.4	1.5	25.65	[8] MWCL'10
0.18-μm CMOS	7.5 (3.1–10.6)	12.7	<-9	n.a.	2.5	2.5–3.9	0.7 @ 1st stage 1.5 @ 2nd stage	13.4	[9] TMTT'11
0.18-μm CMOS	7.5 (3.1–10.6)	13.33	<-10.25	≤-10	2.68	2.68–3.06	1.8	11.8	[10] RWS'12
0.18-μm CMOS	**7.5 (3.1–10.6)**	**13.4**	**<-10**	**<-10**	**3.37**	**3.37-4.39**	**0.4**	**2.4**	**This Work**