A 71-76-GHz Receiver Frontend in 130-nm CMOS

To-Po Wang

Abstract*—A 71-76-GHz receiver frontend with a variable gain range of 48.6 dB is proposed in this paper. The receiver frontend composes of a low-noise amplifier (LNA) and a variable-gain low-noise amplifier (VG-LNA). To achieve high gain and low noise figure, the LNA consists of two common-source stages, and the VG-LNA consists of five common-source stages. Moreover, the gate terminals of the MOSFETs are adjusted to varying the frontend's gain in this work. Based on these methods, a 71-76-GHz receiver frontend has been designed in 130-nm CMOS process. Simulated results confirm these methods applied to this receiver frontend can effectively achieve a high gain of 21 dB at 74 GHz, a variable gain range of 48.6 dB, a minimum noise figure of 6.2 dB at 71 GHz, an input-referred third-order intercept point (IIP_3) of -11.0 dBm. In addition, the receiver frontend is with low supply voltage of 1.3 V.

***Index Terms*—low-noise amplifier (LNA), millimeter-wave (mm-wave), variable-gain low-noise amplifier (VG-LNA),**

I. INTRODUCTION

Because of requirements for wireless high-speed transmission, frequency spectrum from 71 to 76 GHz is opened for wireless local networks by Federal Communications Commission (FCC) [1]. The researches for millimeter-wave (mm-wave) frontend circuits are reported [2]-[12]. For circuits designed and fabricated in 90-nm CMOS [2]-[7], performance of low dc power consumption can be achieved. In [4], a one-stage cascade W-band LNA in 90-nm CMOS operating at 1.8-V supply voltage consumes low dc power of 16 mW. At this bias condition, the LNA deliver the 3.8-dB peak gain at 78 GHz in W band. To enhance the operating frequency beyond 100 GHz, a 3-stage common-source amplifier is designed to achieve this aim [5]. At a supply voltage of 1.0 V with 22-mW dc power, the LNA demonstrates a 3-dB bandwidth from 103 to 105 GHz, and a 9.3-dB peak gain at 104 GHz. To extend the operation frequency, a 3-stage common-source amplifier fabricated in 90-nm CMOS enhances the 3-dB bandwidth to 7 GHz (from 48 to 55 GHz) [7]. The supply voltage and dc power of the LNA is 1.2 V and 30 mW, respectively. At this bias condition, the achieved peak gain is 18 dB at 52 GHz.

For frontend circuits fabricated in 130-nm CMOS, circuits with operation frequency up to mm-wave band are reported [8]-[12]. In [8], two 3-stage common-source amplifiers are reported. The first amplifier achieves 3-dB bandwidth from 34 to 33 GHz. Moreover, it delivers a 19-dB peak gain at 40 GHz, a -18.9-dBm input P_{1dB} at 38 GHz, a -7.4-dBm IIP3, a 1.5-V supply voltage and 36-mW dc power. In addition, the second amplifier achieves 3-dB bandwidth from 51 to 65 GHz. Moreover, it delivers a 12-dB peak gain at 60 GHz, a -9.0-dBm input P_{1dB} at 60 GHz, a 1.5-V supply voltage and 54-mW dc power.

In this paper, a 71-76-GHz receiver frontend in 130-nm CMOS process suitable for the commercial 71 to 76 GHz frequency is proposed. A 2-stage common-source LNA is cascaded with a 5-stage common-source VG-LNA for high gain and wide dynamic gain tuning range. According to the proposed circuit topology, the frontend circuit successfully achieves good performance in terms of bandwidth, gain, noise figure, supply voltage, and gain range.

II. PROPOSED 71-76-GHZ RECEIVER FRONTEND

Fig. 1 shows the functional blocks of the proposed 71-76-GHz receiver frontend. The receiver consists of a low-noise amplifier (LNA), variable-gain low-noise amplifier (VG-LNA), variable-gain mixer, voltage-controlled oscillator (VCO), and variable-gain intermediate-frequency amplifier (VG IF amplifier). As can be seen from Fig. 1, the aim of this work is to design a gain-controllable high-gain LNA.

For the presented functional blocks in Fig. 1, the LNA is the first stage to amplify the millimeter-wave (mm-wave) wireless signal and minimize the noise to improve the signal-to-noise ratio (SNR). To get more insight to the noise performance of a wireless receiver, the Friis equation shown in (1) can be used.

$$NF_{tot} = NF_1 + \frac{NF_2 - 1}{A_{P1}} + \cdots + \frac{NF_m - 1}{A_{P1} \cdots A_{P(m-1)}} \qquad (1)$$

where NF_{tot} is the total noise figure, $NF_{x,\ x=1...m}$ is the noise figure of corresponding stage, $A_{p\ x=1...m-1}$ is the gain of each stage. From (1), it is indicated that the noise performance (NF_{tot}) of a wireless receiver is directly dominated by the first stage (NF_1). In addition, the noise figure of the following stages can be minimized by increasing the gain of previous stages. From Fig. 1, it is observed that the following stage after the LNA is VG-LNA, which is used to adjust the gain of the frontend.

Fig. 2 depicts the circuit schematic of the proposed LNA with VG-LNA. The LNA consists of two common-source stages, and the VG-LNA is with five common-source stages. The tuning voltage (V_{tune}) is connected to gate terminals of the MOSFETs (M_1 to M_7) for gain variation. In addition, thin-film microstrip (TFMS) lines are adopted in this work for signal transmission. The constructed TEMS is composed

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To-Po Wang, Department of Electronic Engineering and Graduate Institute of Computer and Communication Engineering, National Taipei University of Technology, Taipei, Taiwan.

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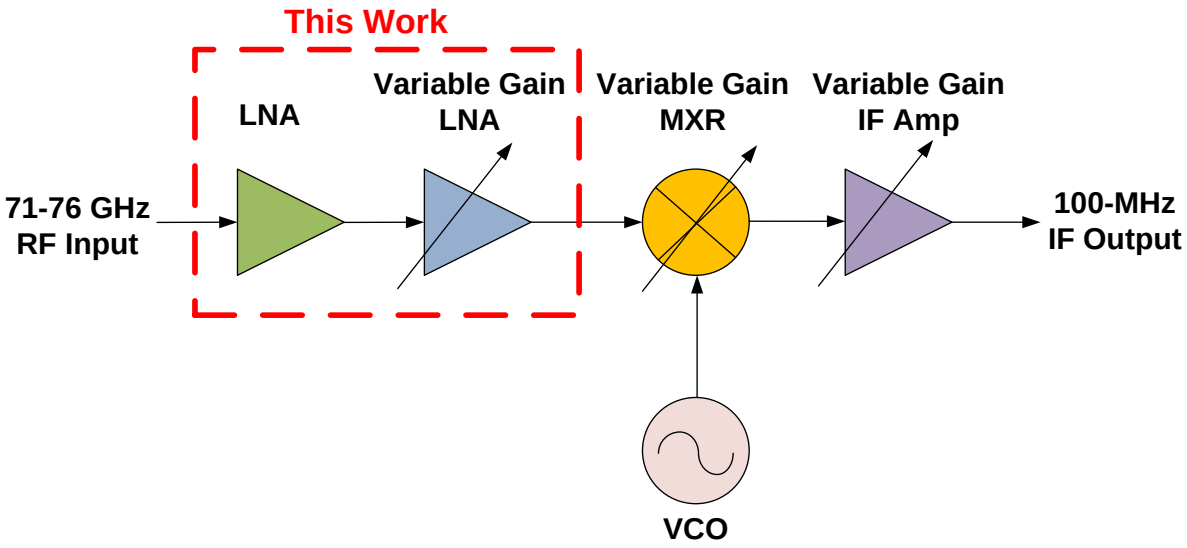

Fig.1.Proposed 71-76-GHz receiver frontend.

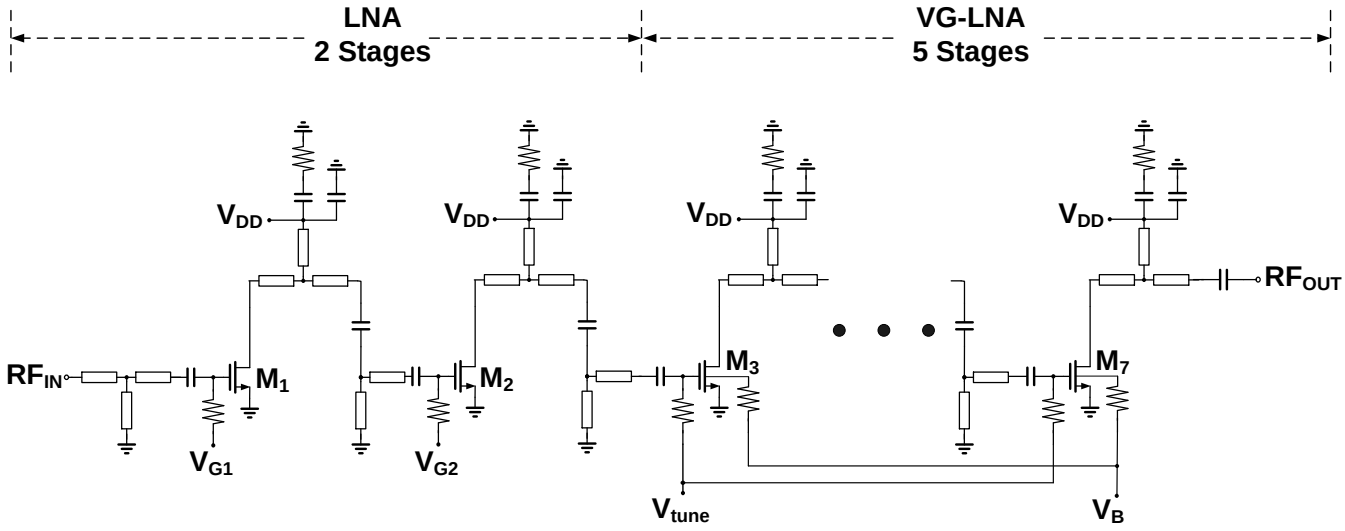

Fig. 2. Schematic of the proposed LNA with VG-LNA.

of the metal 1 (bottom layer) in the 1P8M CMOS process as ground plane and the metal 8 (top layer) as the signal line. The thickness of the dielectric (SiO_2) is 5.7 μm, and almost the propagation signal can be contained in this region. Moreover, the parasitic capacitance between the signal lines and the lossy silicon substrate can be effectively eliminated due to the shielding effects of the ground plane.

III. Simulation Results

The proposed 70-74-GHz receiver frontend has been designed in 130-nm RF CMOS process. The frontend is biased at low supply voltage of 1.3 V, and the total dc power consumption is 70.8 mW. Fig. 3 shows the simulated S parameters of the proposed LNA with VG-LNA. It is observed that the small signal gain is 20 dB from 70 to 74 GHz. Moreover, the peak gain is 21 dB at 74 GHz. Fig. 4 shows the variable gain range of the proposed LNA with VG-LNA. It is found that the gain can be adjusted from 21.6 dB to -27 dB at 74 GHz, resulting in a gain-controlled range of 48.6 dB. Fig. 5 shows the simulated noise figure of the

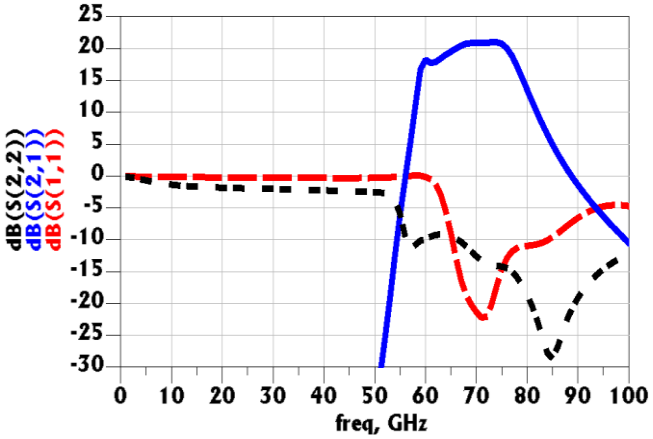

Fig. 3. Simulated S parameters of the proposed LNA with VG-LNA.

proposed receiver frontend. It is indicated that the average noise figure from 70 to 74 GHz is 6.5 dB. In addition, the minimum noise figure is 6.2 dB at 7.1 GHz. To consider the linearity of the proposed LNA with VG-LNA, the simulated input-referred third-order intercept point

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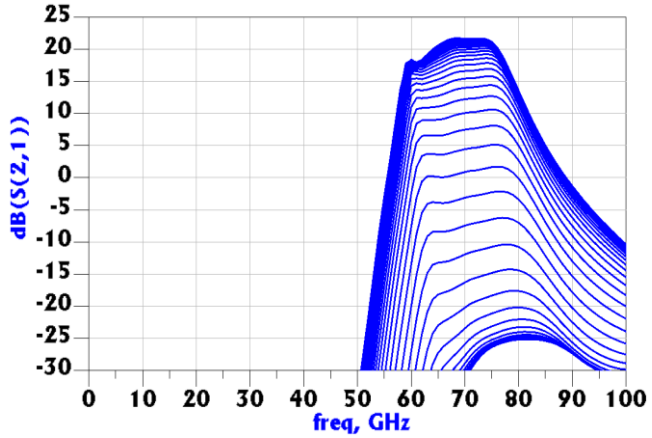

Fig. 4. Simulated variable gain range of the proposed LNA with VG-LNA.

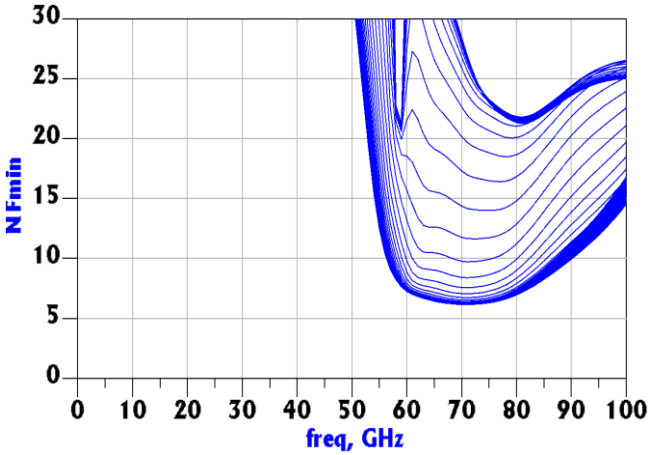

Fig. 5. Simulated noise figure of the proposed LNA with VG-LNA.

(IIP_3) is shown in Fig. 6. The two-tone test is carried out at 74 GHz, and the

frequency spacing is 1 MHz. It is indicated that the IIP_3 for the proposed UWB LNA is -11 dBm. Fig. 7 depicts the simulated gain and output power versus the input power of the proposed LNA with VG-LNA. The one-tone test is carried out at 74 GHz, and the input 1-dB compressed point is -19 dBm.

Table I summaries the circuit performance and compares it to the previously published mm-wave CMOS amplifiers. From this table, it is observed that the proposed circuit can achieves wide 3-dB bandwidth of 15 GHz from 63 to 78 GHz, a high peak gain of 21 dB at 74 GHz, a low noise figure of 6.2 dB at 71 GHz, a low supply voltage of 1.3 V, and a wide variable gain range of 48.6 dB.

IV. Conclusion

A 71-76-GHz receiver fronted using 130-nm CMOS process has been proposed. To achieve high gain and low noise figure, the LNA consists of two common-source stages, and the VG-LNA consists of five common-source stages. Moreover, the gate terminals of the MOSFETs are adjusted to varying the frontend's gain in this work. According to the proposed circuit topology, the frontend circuit successfully achieves good performance in terms of bandwidth, gain, noise figure, supply voltage, and gain range.

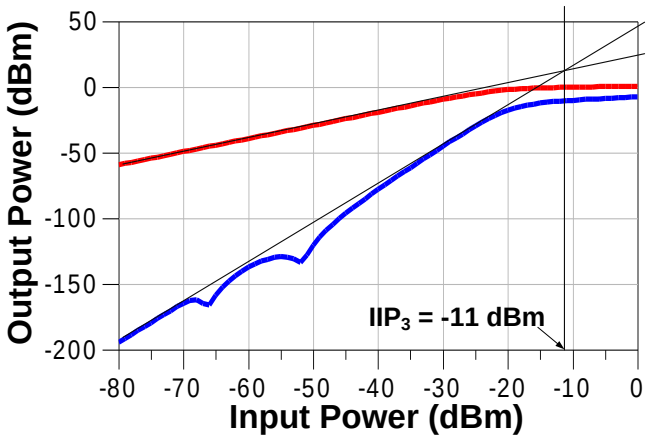

Fig. 6. Simulated input-referred third-order intercept point (IIP_3) of the proposed LNA with VG-LNA.

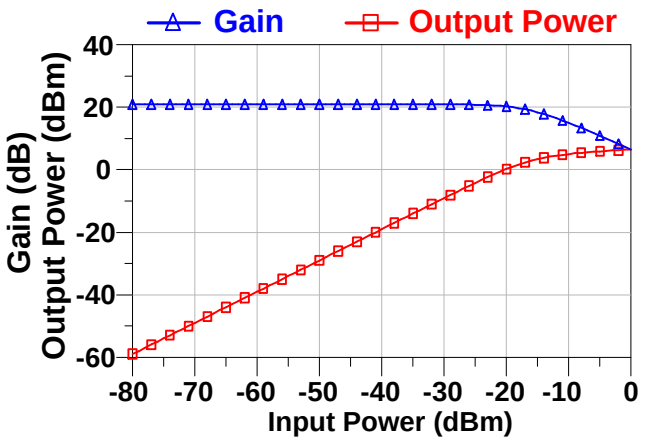

Fig. 7. Simulated gain and output power versus input power of the proposed LNA with VG-LNA.

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Table I. Performance summary and comparison to the previously published millimeter-wave CMOS amplifier

Process	3-dB BW (GHz)	Peak Gain (dB)	NF (dB)	Input P_{1dB} (dBm)	IIP3 (dBm)	Supply Voltage (V)	DC Power (mW)	Gain Control (dB)	Topology	Ref.
90-nm CMOS	12 (32-44)	7.3 at 35 GHz	n.a.	-12 at 40 GHz	n.a.	1.5	19	w/o	2-stage Common Source	[2] RFIC'04
90-nm CMOS	5 (55-60)	14.6 at 58 GHz	4.5	-14.1 at 58 GHz	-6.8	1.5	24	w/o	2-stage Cascode	[3] RFIC'06
90-nm CMOS	> 30	3.8 at 78 GHz	n.a.	n.a.	n.a.	1.8	16	w/o	1-stage Cascode	[4] CSIC'06
90-nm CMOS	> 18	4.8 at 94 GHz	n.a.	n.a.	n.a.	1.8	30	w/o	2-stage Cascode	[4] CSIC'06
90-nm CMOS	> 11	1.65 at 92 GHz	n.a.	n.a.	n.a.	1.5	34.5	w/o	Transformer Coupled Cascode	[4] CSIC'06
90-nm CMOS	2 (103-105)	9.3 at 104 GHz	n.a.	n.a.	n.a.	1.0	22	w/o	3-stage Common Source	[5] ISSCC'07
90-nm CMOS	5 (71-76)	14 at 72.5	n.a.	-13 at 72 GHz	n.a.	2.0	36	30 (Current Steering)	3-stage Cascode	[6] RFIC'08
90-nm CMOS	7 (48-55)	18 at 52 GHz	n.a.	n.a.	n.a.	1.2	30	w/o	3-stage Common Source	[7] IMWS'12
130-nm CMOS	10 (34-44)	19 at 40 GHz	n.a.	-18.9 at 38 GHz	-7.4	1.5	36	w/o	3-stage Cascode	[8] JSSC'05
130-nm CMOS	14 (51-65)	12 at 60 GHz	8.8 at 60 GHz	-9 at 60 GHz	n.a.	1.5	54	w/o	3-stage Cascode	[8] JSSC'05
130-nm CMOS	10 (34-44)	20 at 43 GHz	6.3 at 41 GHz	-12.5 at 40 GHz	-3.0	1.5	36	w/o	3-stage Common Source	[9] MWCL'06
130-nm CMOS	5 (51-56)	24.7 at 56 GHz	7.1 at 56.8 GHz	-22 at 56 GHz	n.a.	2.4	72	w/o	3-stage Cascode	[10] ISSCC'06
130-nm CMOS	21 (42-63)	18.1 at 45 GHz 17.8 at 60 GHz	8.2 at 60 GHz	-16.5 at 60 GHz	n.a.	2.4	91.2	w/o	4-stage Cascode	[11] IMS'07
130-nm CMOS	9 (71-80)	7.0 at 75 GHz	n.a.	-13.4 at 75 GHz	n.a.	1.8	59	w/o	4-stage Common Source	[12] MWCL'07
130-nm CMOS	**15 (63-78)**	**21 at 74 GHz**	**6.2 at 71 GHz**	**-19 at 74 GHz**	**-11.0**	**1.3**	**70.8**	**48.6 (Gate Bias & Body Bias)**	**2-stage CS LNA wi 5-stage CS VG-LNA**	**This Work (Simu.)**