A Comparative Study of Back Gate Misalignment Effects for Nano Scale Symmetric and Asymmetric Double Gate Mosfets

Ralesh Ranjan Biswal, Pradipta Dutta

Abstract*— The technical advancement in the field of device scaling leads to a major concern i.e. short channel effects in conventional single gate (SG) Metal- Oxide-Semiconductor Field-Effect-Transistor (MOSFET). Hence the double gate (DG) MOSFETs become a best option due to its better controllability of gate over the both the front and back channel. Primarily there are two types of DG-MOSFETs, known as Symmetric DG-MOSFET and Asymmetric DG-MOSFET. But the misalignment of top gate and bottom gate is a matter of concern in the fabrication process of the device. This misalignment of both the gates can cause damage to the device characteristics and affect the parameters like threshold voltage, drain current and surface potential. In this paper the back gate misalignment effects are investigated for both symmetric and asymmetric DG-MOSFETs and a comparative study has been made. The misalignment is considered towards both source side and drain side. Quantum mechanical effect and mobility degradation are not incorporated in our work for simplicity purpose.

Index Terms*— DG MOSFET, Gate Misalignment, Threshold voltage roll off, Drain current degradation, Surface potential variation

I. INTRODUCTION

In the past few years, the device scaling has advanced to a remarkable level in the field of Very Large Scale Integration (VLSI). But in the sub-40nm region, single gate MOSFET exhibits short channel effects such as threshold voltage roll off, drain induced barrier lowering (DIBL), hot carrier effect and many more. To overcome these effects multi-gate MOSFETs are introduced. DG-MOSFETs are one of the most promising one among them. The presence of both front gate and back gate provides better control over channel and results in reduction in short channel effects. DG MOSFET has reduced transistor count and improved performance for logic [1]-[3]. But there is a possibility of top and bottom gate misalignment during the fabrication process. This misalignment can lead to the device parameters to be varied and can cause damage to the device characteristics. The misalignment can happen either side of the gate i.e. drain side or source side. It has been observed that gate misalignment effect becomes a major problem with shrinking the device dimension. Previous works have shown the gate misalignment effects on DG MOSFET in sub-80nm region and it has shown That the threshold voltage is not affected whether the back gate exists or not [4]. In this work we investigated the device behavior of DG-MOSFET with bottom gate misaligned for 20nm region and the effects on various parameters is studied for both symmetric and asymmetric DG-MOSFET. For simplicity, quantum mechanical effect and mobility degradation is not incorporated in our work. The DG-MOSFET device is designed in Sentaurus TCAD simulator.

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II. DG-MOSFET STRUCTURE

The concept of device scaling has tremendously resulted in better device density and performance. As the downscaling of CMOS technology approaches physical limitations, the need for alternative device structure arises. One such structure is Double-Gate MOSFET [5]. The key theme of a DG-MOSFET is to have a channel of scaled width and to manage that channel, gate contacts are given to both the sides i.e. front and back side. The two types of gates namely the front gate and back gate in DG-MOSFET can be independently driven to reduce the power consumption and improve the performance of the device [6]. DG-MOSFET devices are otherwise known as scalable silicon transistors because of its better control of the short-channel effects in the double-gate structure [7]. In a DG-MOSFET when two gates are coupled with each other, then it reduces the short channel effects and leakage current. The double gate transistors are operated with very small input voltage in comparison to the existing CMOS transistors which in terms indicate reduced power consumption [8]. There are four different kinds of DG-MOSFET designs are available such as the tied symmetric and asymmetric double gates, and the separated symmetric and asymmetric double gates as shown in Fig. 1. In the tied structure, the two gates are supplied with same potential and on the contrary in the separated structure, both gates are supplied with different potentials.

III. GATE MISALIGNMENT EFFECTS

Misalignments of front gate and back gate are the major issues during fabrication. The DG MOSFET behaves as a conventional single gate MOSFET because some part of channel has one gate due to misalignment. The misalignment can be happened either side of the device; i.e. drain side (DSM) or source side (SSM). Due to this gate misalignment, the device characteristics degrades. The parameters like threshold voltage, drain current are degraded when the gate misalignment takes place. Furthermore due to absence of electric field, electrostatic control over channel reduces [9]

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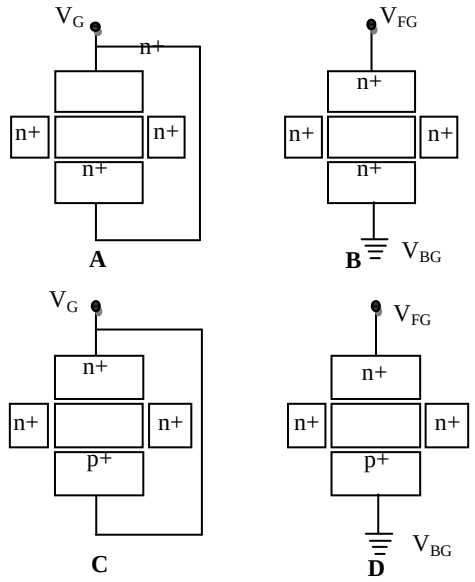

Figure 1. Schematics of various types of DG-MOSFETs (A) Symmetric Tied DG-MOSFET, (B) Symmetric Independent DG-MOSFET, (C) Asymmetric Tied DG-MOSFET, (D) Asymmetric Independent DG-MOSFET [8].

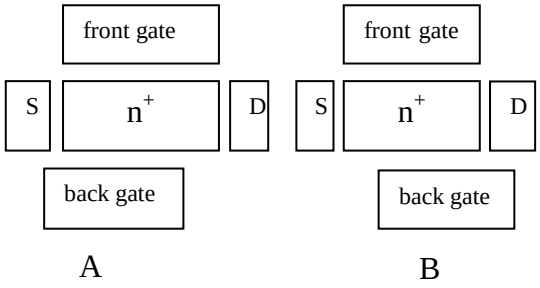

Figure 2. Schematics of gate misalignments (A) Source Side Misalignment (SSM) and (B) Drain Side

IV. SIMULATION RESULTS AND DISCUSSION

In this work we designed symmetric and asymmetric DG MOSFET on Sentaurus TCAD simulator [10]. Front gate oxide and back gate oxide are taken to be 2nm of thickness. The Silicon film thickness is taken to be 20nm. The source and drain are of constant doping with doping concentration of 10^{18} cm^{-3}. The doping concentration for substrate is taken to be 10^{16} cm^{-3}. The back gate misalignment of 4nm, 6nm and 8nm are taken on both source and drain sides. The variation in device parameters are compared for gate misalignment in symmetric and asymmetric condition.

A. Comparison of Threshold Voltage Variation

When the gate is misaligned towards the source side the control of gate over the channel is reduced yields a corresponding degradation of on current resulting an increment in threshold voltage occurs for asymmetric DG-MOSFET [4]. The misalignment of back gate towards source side weakens the back channel and hence increment in threshold voltage happens. However for symmetric DG-MOSFET, as the back gate is biased with same amount of voltage as that of front gate, the control of back gate over the back channel increases. For the back gate misalignment towards either side i.e. source side or drain side the control of back gate persists and relatively small increment in threshold voltage occurs than that for asymmetric DG-MOSFET. From Figure-3 and Table-1 the variation in threshold voltage for drain side misalignment for both symmetric and asymmetric DG-MOSFET is observed and from Figure-4 and Table-2 threshold voltage for source side misalignment for both symmetric and asymmetric DG-MOSFET is observed.

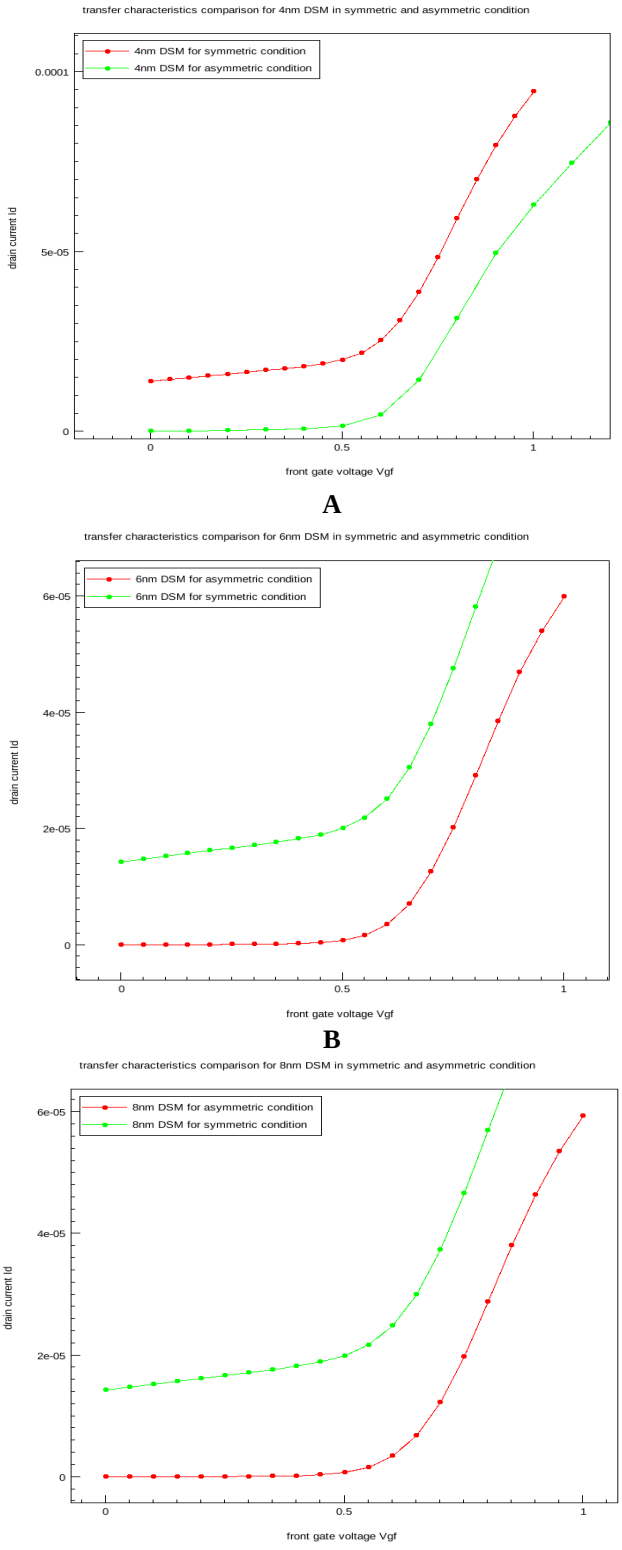

Figure-3 (A) Comparison of transfer characteristics for 4nm DSM in symmetric and asymmetric condition (B) Comparison of transfer characteristics for 6nm DSM in symmetric and asymmetric condition (C) Comparison of transfer characteristics for 8nm DSM in symmetric and asymmetric condition

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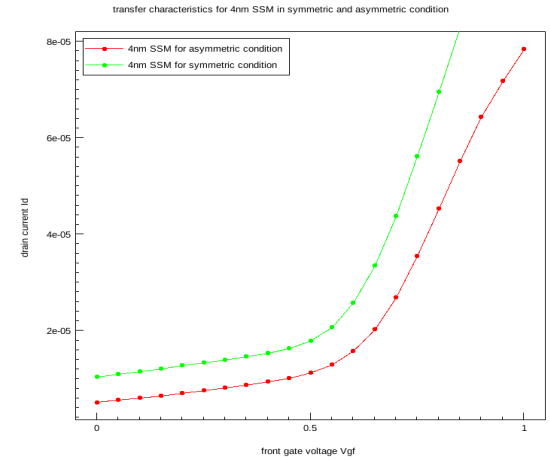
TABLE-1 Variation in Threshold Voltage For Different Drain Side Misalignment For Symmetric And Asymmetric Condition

Drain Side Misalignment (DSM) in nm	Threshold voltage for symmetric condition	Threshold voltage for asymmetric condition
4nm	0.528V	0.624V
6nm	0.532V	0.632V
8nm	0.534V	0.638V

From Table-1 it is observed that for drain side misalignment (DSM) for symmetric DG-MOSFET exhibits a less variation in threshold voltage than that of asymmetric DG-MOSFET.



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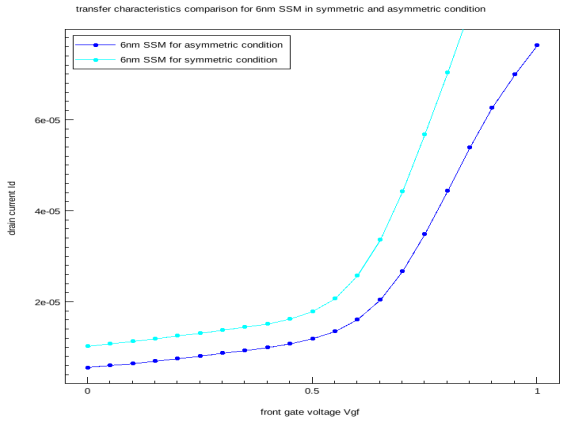

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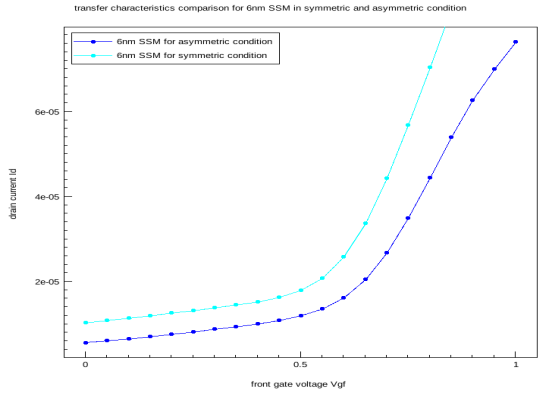

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Figure-4 (A) Comparison of transfer characteristics for 4nm SSM in symmetric and asymmetric condition (B) Comparison of transfer characteristics for 6nm SSM in symmetric and asymmetric condition (C) Comparison of transfer characteristics for 8nm SSM in symmetric and asymmetric condition.

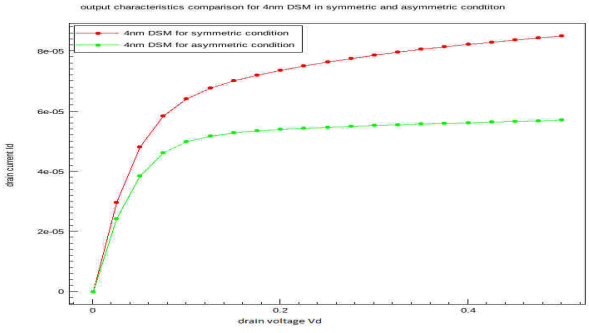
TABLE-2 Variation In Threshold Voltage For Different Source Side Misalignment (Ssm) In Symmetric And Asymmetric Condition.

Source Side Misalignment in nm	Threshold voltage for symmetric condition	Threshold voltage for asymmetric condition
4nm	0.540V	0.558V
6nm	0.542V	0.560V
8nm	0.544V	0.563V

From Table-2 it is found that the threshold voltage increases more for asymmetric DG-MOSFET compared to symmetric DG-MOSFET for different source side misalignment (SSM).

B. Comparison of Drain Current Degradation

Previously it has been found that for asymmetric DG-MOSFET the drain current degradation is more for either side misalignment i.e. for drain side misalignment and source side misalignment [4]. Now for symmetric DG-MOSFET, as the back gate is biased with some amount of voltage which is equal as of front gate, the back gate controls the channel in a better manner compared to an asymmetric one. Though for the back gate misalignment towards either side i.e. drain side or source side, the gate control over the back channel exxists to some extent. So the drain current degradation also becomes less for symmetric DG-MOSFET comparing asymmetric DG-MOSFET as observed from Figure-5 and Figure-6.



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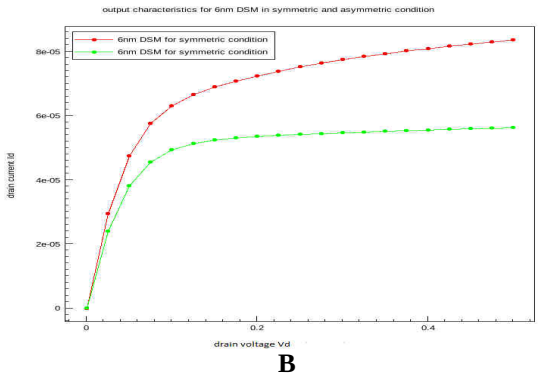

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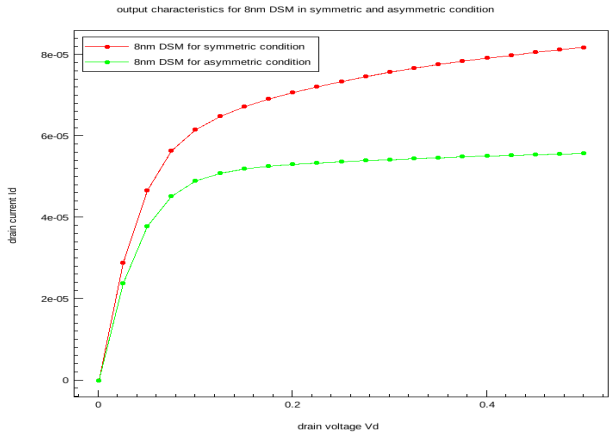

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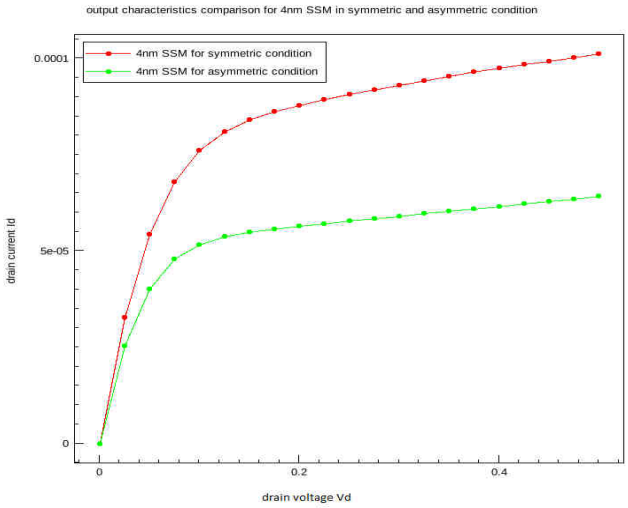
Figure-5 (A) Comparison of output characteristics for 4nm DSM in symmetric and asymmetric condition (B) Comparison of output characteristics for 6nm DSM in symmetric and asymmetric condition (C) Comparison of output characteristics for 8nm DSM in symmetric and asymmetric condition

TABLE-3 Comparison of Drain Current For Different Source Side Misalignment (Ssm) In Symmetric And Asymmetric Condition

Drain Side Misalignment in nm	Drain current for symmetric condition	Drain Current for asymmetric Condition
4nm	94.6μA	63.10 μA
6nm	92.5 μA	60.03 μA
8nm	90.6 μA	59.40μA

From Table-3 it is observed that the drain current gradually decreases for more misalignment towards drain side in both symmetric and asymmetric DG-MOSFET. But for asymmetric DG-MOSFET the drain current value is much less as compared to symmetric one. The reason behind it is, better gate controllability of symmetric DG-MOSFET provides drain current to degrade to a lesser extent.



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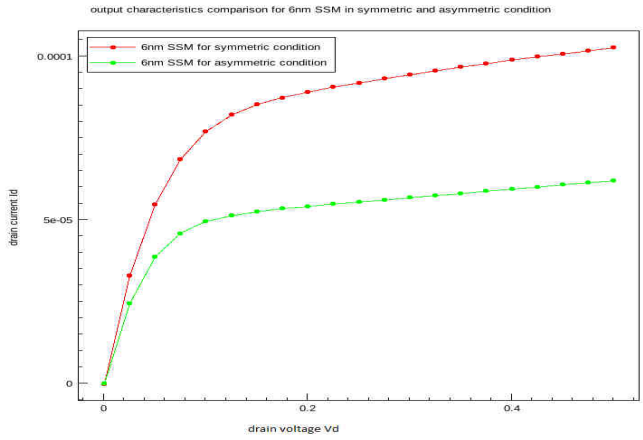

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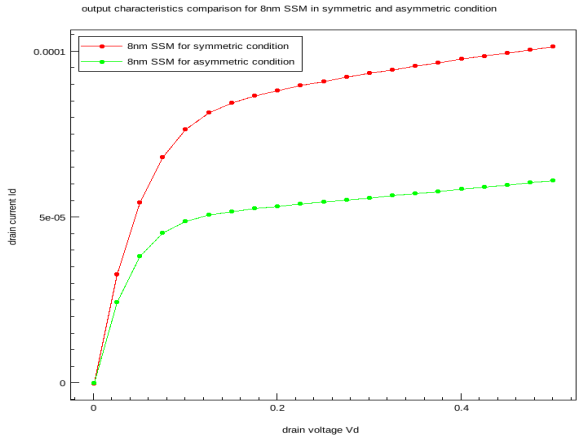

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Figure-6 (A) Comparison of output characteristics for 4nm SSM in symmetric and asymmetric condition (B) Comparison of output characteristics for 6nm SSM in symmetric and asymmetric condition (C) Comparison of output characteristics for 8nm SSM in symmetric and asymmetric condition.

TABLE-4 Comparison Of Drain Current For Different Source Side Misalignment For Symmetric And Asymmetric Condition

Source Side Misalignment in nm	Drain current for symmetric condition	Drain current for asymmetric condition
4nm	0.193mA	78.2μA
6nm	0.182mA	76.3 μA
8nm	0.171mA	75.2 μA

From Table-4 it is found that the drain current degrades more for source side misalignment in asymmetric condition than in symmetric one. Better gate control in symmetric DG-MOSFET ensures that the degradation in drain current is less than compared to asymmetric DG-MOSFET.

C. COMPARISON OF SURFACE POTENTIAL VARIATION

From Figure-7, it is observed that for the drain side misalignment in asymmetric DG-MOSFET, the front surface potential decreases as compared to symmetric DG-MOSFET.

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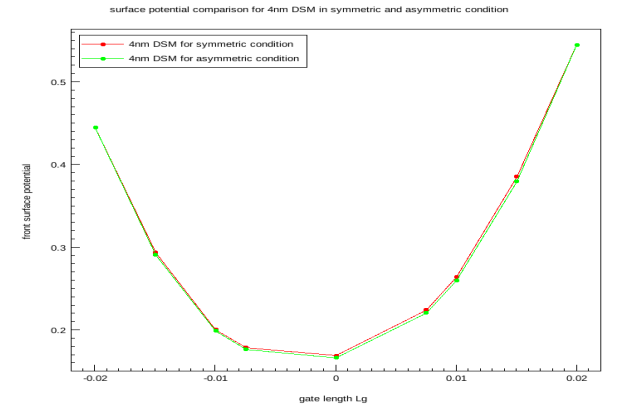
The more decrement in front surface potential also happens for source side misalignment in asymmetric DG-MOSFET than the symmetric DG-MOSFET as observed from Figure-8. As for symmetric DG-MOSFET the back gate has same amount of voltage, it creates an impact on the electric field and leads to less decrement in front surface potential even for the back gate misalignment. For the misalignment of back gate either source or drain side, fringing field effect exhibits a significant role on the front surface potential[11].Larger back gate misalignment lowers more the front surface potential due to stronger electric field effects.



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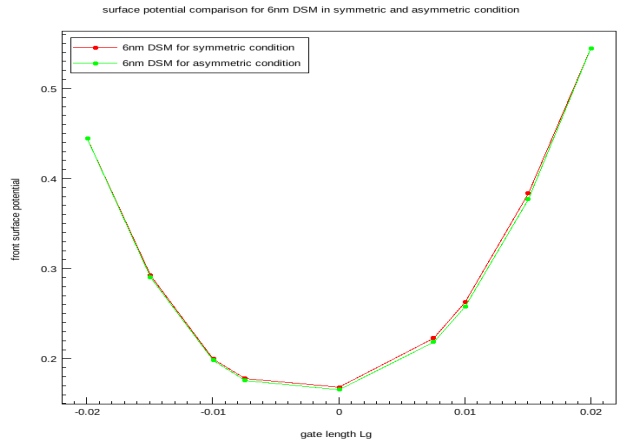

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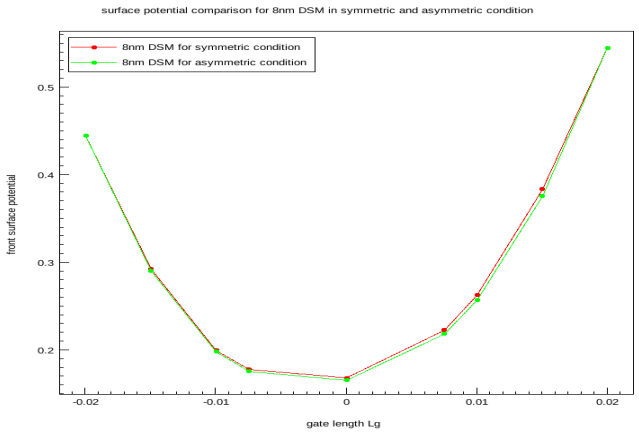

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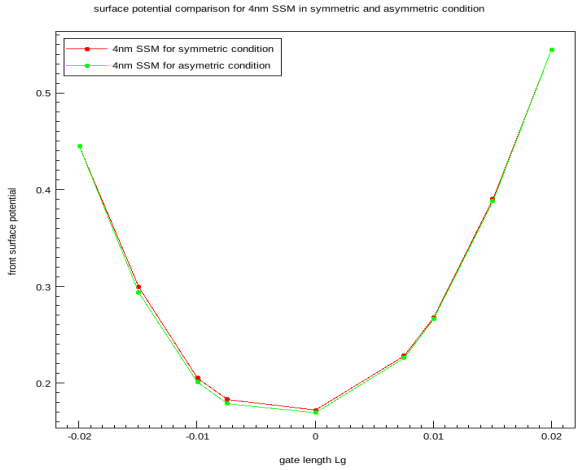
Figure-7 (A) Comparison of front surface potential for 4nm DSM in symmetric and asymmetric condition (B) Comparison of front surface potential for 6nm DSM in symmetric and asymmetric condition (C) Comparison of front surface potential for 8nm DSM in symmetric and asymmetric condition



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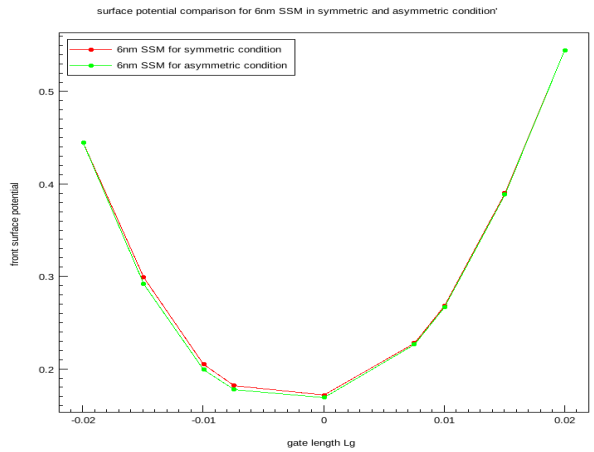

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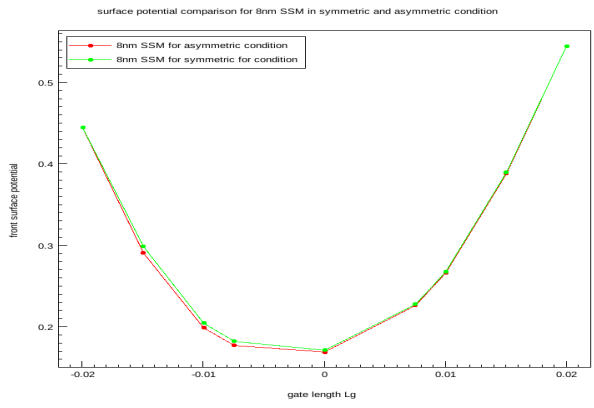

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Figure-8 (A) Comparison of front surface potential for 4nm SSM in symmetric and asymmetric DG-MOSFET (B) Comparison of front surface potential for 6nm SSM in symmetric and asymmetric DG-MOSFET (C) Comparison of front surface potential for 8nm SSM in symmetric and asymmetric DG-MOSFET.

From Figure-9 it can be observed that the surface potential decreases more for drain side misalignment (DSM) than for source side misalignment (SSM) in symmetric condition, same as that of asymmetric one.

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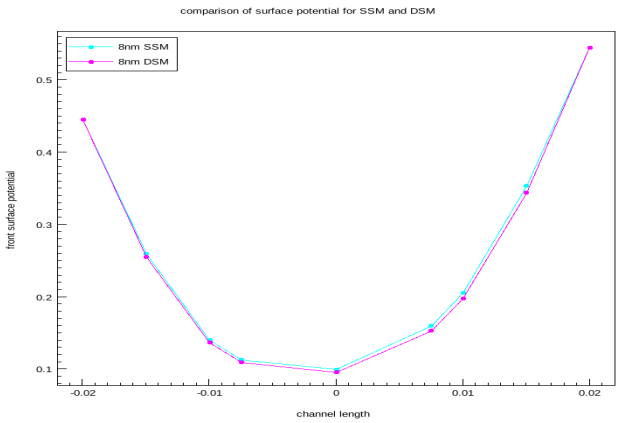

Figure-9 Comparison of front surface potential for 8nm DSM and SSM in symmetric condition

V. CONCLUSION

In the present work, the effects of gate misalignment have been investigated in the DG MOSFET structures by using Sentaurus TCAD device simulator. For the back gate misalignment towards source and drain side for asymmetric DG-MOSFET, the threshold voltage increases and so as the leakage current . There is a degradation in drain current, which is observed from the output characteristics. It also shows that the device suffers short channel effect for source side misalignment (SSM) than for drain side misalignment (DSM) for asymmetric DG-MOSFET. Also for the symmetric DG-MOSFET the back gate misalignment effect is compared with that of asymmetric one. It has been found that the asymmetric DG-MOSFET suffers more increment in threshold voltage, hence the leakage current, more degradation in drain current and also more decrement in surface potential when the gate is misaligned for either source side or drain side. For symmetric DG-MOSFET the back gate, biased with same amount of voltage that of front gate, shows a better control over the channel even for the misalignment of gate towards either side of it.

REFERENCES

1. Mahmoodi, H., Mukhopadhyay, S., Roy, K., 2004. High performance and low power domino logic using independent gate control in double-gate SOI MOSFETs, in Proc. IEEE Int. SOI Conf., 2004, pp. 67–68.
2. Jente, B., Kuang, Keunwoo Kim, Ching-Te Chuang, Hung C. Ngo, Fadi H. Gebara, and Kevin J. Nowka, 2008. Circuit Techniques Utilizing Independent Gate Control in Double-Gate Technologies, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 16, No. 12, pp. 1657-1665.
3. Mukhopadhyay, S., Mahmoodiand, H., Roy, K., A Novel High Performance and Robust Sense Amplifier Using Independent Gate Control in Sub-50-nm Double-Gate MOSFET, 2006. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 14, No. 2, pp. 183-192.
4. Shen, J., Man, T., Chan, M., 2D Analysis of Bottom Gate Misalignment and Process Tolerant for Sub- 100nm Symmetric Double-Gate MOSFETs, 2003. Electron Devices and Solid-State Circuits.
5. http://en.wikipedia.org/wiki/Multigate_device.
6. Nowak, E., et.al, Turning Silicon on its edge, 2004. IEEE circuits and Device Magazine, pp.20-31.
7. Jin-Woo Han, Chung-Jim Kim, and Yang-Kyu Choi, Universal Potential Model in Tied and Separated Double-Gate MOSFETs with consideration of symmetric and asymmetric structure, 2008. IEEE Transaction on Electron Devices Vol.-55, No.-6, pp. 1472-1479.
8. Shrivastava, A.K., Akashe, S., Design high performance and low power 10T full adder using Double Gate MOSFET at 45nm technology,2013. ICCCCM, pp.1-5.
9. Sarangi, S., Gopi Krishna .S, Santra, A., Shiv Bhushan, and Tiwari, P.K., A Simulation-based Study of Gate Misalignment Effects in Triple-Material Double Gate (TM DG) MOSFETs. 2013. IEEE conference, IMAC4S, pp.4
10. "Integrated Systems Engineering (ISE) TCAD Manuals," Integr.Syst. Eng., Zurich, Switzerland, 2006. Release 10.0. International Technology. entaurus TCAD simulator.
11. Kuo, J.B.; Sun, E.C., "A compact threshold voltage model for gate misalignment effect of DG FD SOI nMOS devices considering fringing electric field effects," Electron Devices, IEEE Transactions on , vol.51, no.4, pp.587,596, April 2004.

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