A High-P_{SAT} High-OP_{1dB} 60-GHz Power Amplifier with Miniature Marchand Balun and Non-Uniform-Offset Coupler in 90-nm CMOS

To-Po Wang, Wei-Qing Xu

Abstract—A high-P_{SAT} high-OP_{1dB} 60-GHz power amplifier (PA) with miniature Marchand balun and non-uniform-offset 90• coupler in 90-nm CMOS is proposed in this paper. The PA is constructed with a four-way structure, and each way consists of a three-stage cascode device. In order to improve the gain, output power (Pout), and power-added efficiency (PAE), the cross-coupled pairs are adopted in this PA. Moreover, a minimized Marchand balun is proposed to minimize the circuit area. Furthermore, a non-uniform-offset 90• coupler is proposed to improve the signal imbalance. Based on these methods, a 60-GHz PA has been designed in 90-nm CMOS process. Simulated results confirm these methods applied to this PA can effectively improve the circuit performance in terms of gain, Pout, PAE, and power density (Saturated output power (P_{SAT})/Area).

Index Terms—output power (Pout), power amplifier (PA), power-added efficiency (PAE), saturated output power (P_{SAT}).

I. INTRODUCTION

Due to the 60-GHz band has been planned for Industrial, Scientific, and Medical (ISM) by Federal Communications Commission (FCC) [1]. The requirements on high-speed wireless communication and developments of millimeter-wave (mm-wave) power amplifiers were accelerated [2]-[7]. In order to improve PA performance, the cross-coupled pair, miniature Marchand balun, and non-uniform-offset 90° coupler are proposed and introduced in this work.

II. PROPOSED PA

Fig. 1 shows the schematic of the proposed 60-GHz power amplifier. This PA is with the four-way structure, and each way consists of three-stage cascode devices. In order to achieve maximum output power, all the transistors are 38 fingers with 4-□m unit finger width. To have sufficient current-handling capacity and to overcome the lossy silicon substrate, the thin-film microstrip (TFMS) lines are adopted at this design. By using the 1P9M CMOS process, the TFMS line was composed of metal1 (bottom layer) as ground plane and metal9 (top layer) is as the signal line.

The major difficulties for designing a CMOS power amplifier are low gain, low output power (Pout), and low PAE.

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In order to alleviate these difficulties, the cross-coupled pairs are adopted in this design [8], as shown in Fig. 1. For a conventional PA, the power-added efficiency (PAE) can be expressed as [8]

$$PAE\_PA_{conv}(\%) = \frac{P_{out} - P_{in}}{P_{DC}} \times 100 \qquad (1)$$

where P_{in} is the input power, P_{out} is the output power, and P_{DC} is the dc power dissipation. For the proposed PA, the required input power (P_{in}) to achieve the same output power (P_{out}) can be reduced to ($P_{in} - A_p$) due to the cross-coupled pair, and the A_p is the enhanced gain. For the proposed PA, the PAE can be formulated as

$$PAE\_PA_{propopsed}(\%) = \frac{P_{out} - \left(P_{in} - A_p\right)}{P_{DC}} \times 100 \quad (2)$$

From (2), it is observed that the PAE of the proposed PA is higher than that (1) of the counterpart without a cross-coupled pair.

In the design of an on-chip 180°hybrid, the Marchand balun [9] is widely used as the 180°hybrid due to its excellent amplitude and phase match. Fig. 2(a) shows the structure of a conventional Marchand balun, which is constructed by broadside-coupled lines. The dimension is 108 □m x 51 □m. In order to reduce the chip size of the conventional Marchand balun, the miniature Marchand balun is proposed in Fig. 2(b). The dimension of the proposed miniature Marchand balun is 62 □m x 28 □m, which is much smaller (31.5%) than the conventional one.

Fig. 3 (a) and (c) shows the simulated and measured insertion loss and amplitude/phase imbalance of the conventional Marchand balun, respectively [9]. Fig. 3 (b) and (d) shows the simulated insertion loss and amplitude/phase imbalance of the proposed miniature Marchand balun, respectively. From Fig. 3(a) and (b), it is observed that the proposed miniature Marchand balun is with similar performance to the conventional one in terms of insertion loss. From Fig. 3(c) and (d), it is also shown that the proposed miniature Marchand balun is with similar performance to the conventional one in terms of amplitude/phase imbalance.
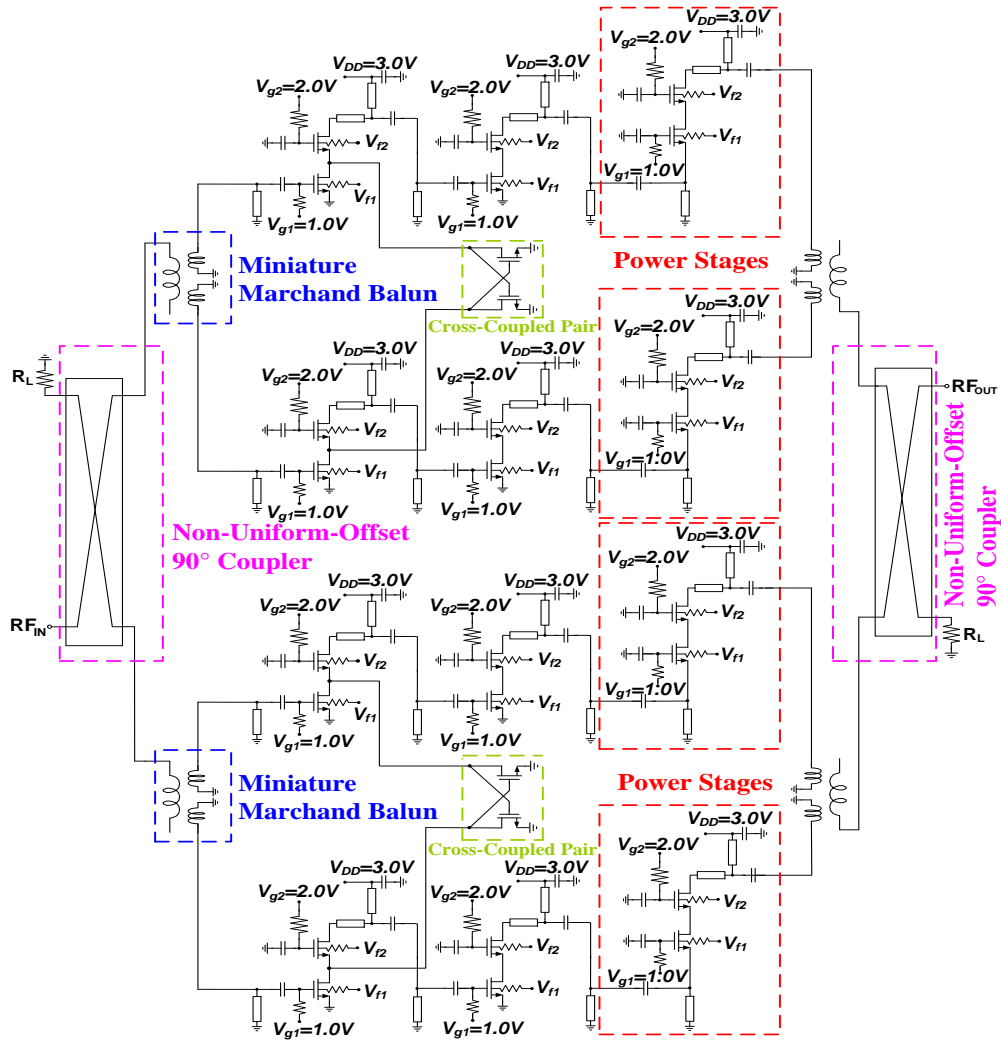
Fig. 1. Circuit schematic of the proposed 60-GHz power amplifier.

From Fig. 2, the chip area of the proposed miniature Marchand balun is only 31.5% of the conventional one. In addition, the performance of the proposed miniature Marchand balun is similar to that of the conventional one. Therefore, the proposed miniature Marchand balun is quite suitable for mm-wave circuit applications.
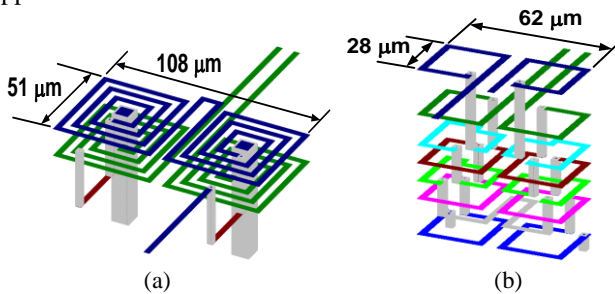

Fig. 2. (a) Conventional Marchand balun and (b) proposed miniature Marchand balun.

The required on-chip 90° hybrid for this work is implemented by using broadside-coupled lines. The widely used conventional uniform-offset 90° coupler is shown in Fig. 4(a). This uniform-offset 90° coupler is meandered to achieve a compact layout [9], and there is additional 1-□m uniform offset between the metals for reducing the coupling coefficient. Fig. 5(a) shows the simulated results of the conventional uniform-offset 90° coupler. It is observed that

there is a 2-dB difference between the S21 and S31 at the center frequency. In order to reduce the difference, the non-uniform-offset 90° coupler is proposed in Fig. 4(b). Fig. 5(b) shows the simulated results of the proposed non-uniform-offset 90° coupler. It is observed that the S21 and S31 are with the same coupling around 60 GHz. Therefore, the proposed non-uniform-offset 90° coupler can provide more balanced signals than that of the conventional one.
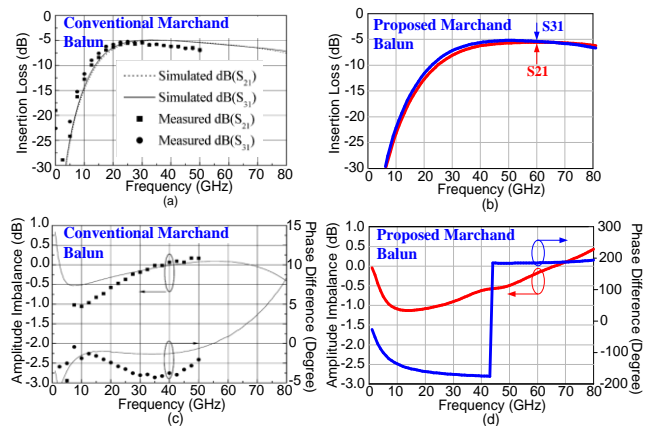

Fig. 3. Simulated insertion losses of (a) conventional Marchand balun [9] and (b) proposed miniature Marchand balun. Simulated amplitude and phase imbalance of (c) conventional Marchand balun [9] and (d) proposed miniature Marchand balun.
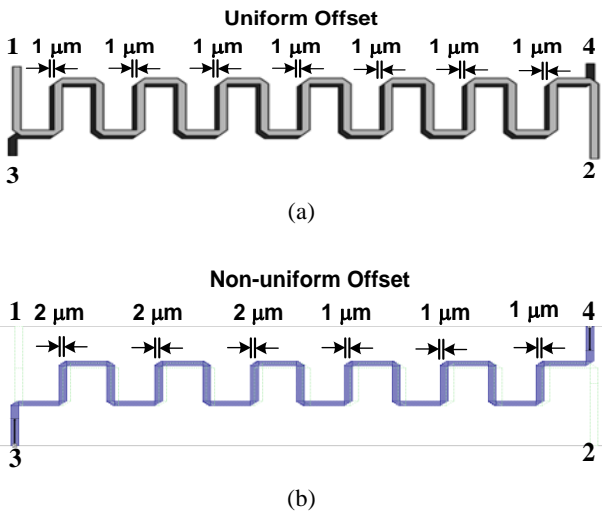
(a)

(b)

Fig. 4. (a) Conventional uniform-offset 90° coupler and (b) proposed non-uniform-offset 90° coupler
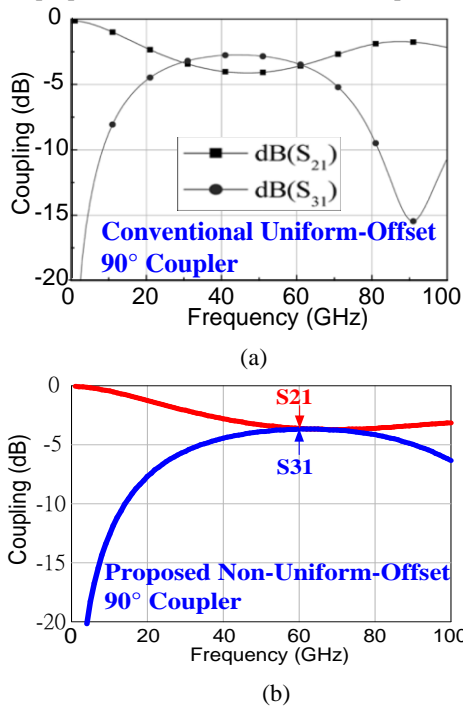

(a)

(b)

Fig. 5. Simulated results of the (a) conventional uniform-offset 90° coupler [6] and (b) proposed non-uniform-offset 90° coupler.

III. SIMULATION RESULTS

The proposed 60-GHz PA has been designed in 90-nm RF CMOS process. Fig. 6 shows the chip layout this PA. The chip size without pads is 0.7 x 0.7 mm^2. The supply voltage (V_{DD}) of this PA is 3.0 V, and the dc current of each way (PA unit) is 198 mA. The current density has been taken into account according to the foundry's layout rules. The simulation is performed by using circuit simulator Agilent's Advanced Design System (ADS) software. The on-chip passive components including transformers, inductors, capacitor, and interconnections are simulated by using full-wave electronic-magnetic (EM) simulation tool, Sonnet and HFSS.

Fig. 7(a) shows the simulated S parameters (with EM simulation) of the proposed 60-GHz PA with and without the cross-coupled pair. The device size of the cross-coupled transistors is 24 □m /0.1 □m. It is indicated that the peak gain of S21 can be effectively increased from 11.6 dB to 15.0

dB. Fig. 7(b) shows the simulated gain and output power versus input power (with EM simulation) of the proposed PA with and without the cross-coupled pair. The simulated gain and output power for the proposed PA with cross-coupled pair is carried out at 63.2 GHz. From Fig. 7(b), it is observed that the gain and output power of the proposed PA can be improved due to the cross-coupled pair. The P$_{SAT}$ and OP1dB of the proposed PA are 22.0 dBm and 17.8 dBm, respectively.
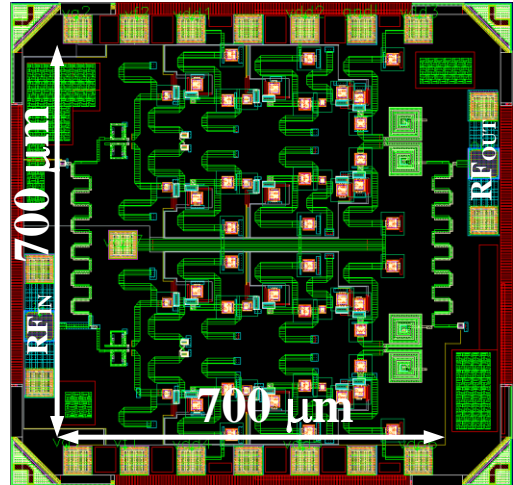

Fig. 6. Chip layout of the proposed fully integrated 60-GHz PA
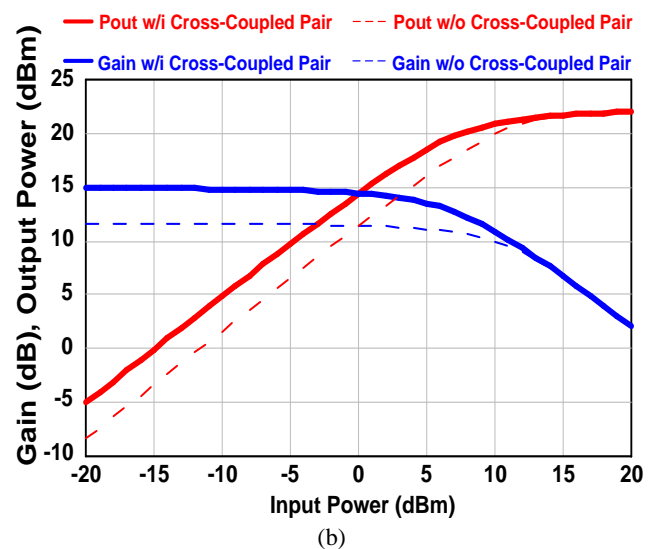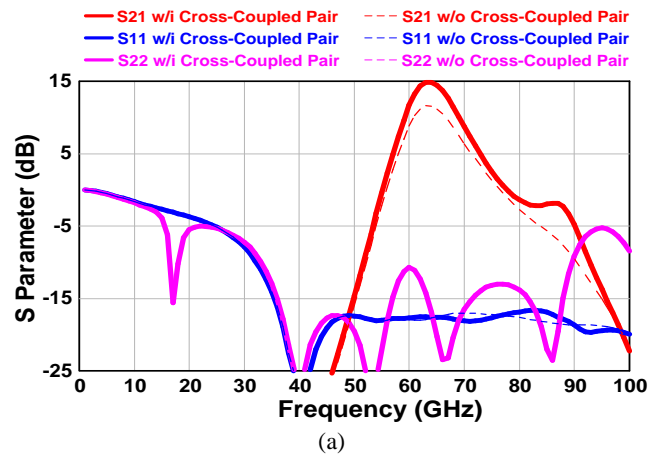

(a)

(b)

Fig. 7. (a) Simulated S parameters of the proposed PA (after EM simulation) with and without the cross-coupled pair. Note that the S22 of the PA w/i and w/o cross-coupled pair are coincided. (b) Simulated gain and output power versus input power (after EM simulation) with and without the cross-coupled pair.

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Table I. Performance summary of the recently published 60-GHz CMOS PAs

| Process	Freq. (GHz)	P_{SAT} (dBm)	OP1dB (dBm)	Gain (dB)	Area (mm^2)	P_{SAT}/Area (mW/mm^2)	Topology	Ref.
90-nm CMOS	60	10.6	8.2	8.3	n.a.	n.a.	3-stage common-source	[11] ISSCC'08
90-nm CMOS	60	12.6	8.8	10	0.64	28.43	3-stage common-source	[12] RFIC'09
90-nm CMOS	60	14.5	10.5	26.1	0.64	44.04	DAT combing + 3-stage cascode	[10] MTT'09
		18	14.5	26.6	0.64	99.00		
90-nm CMOS	60	13.8	10.3	30	0.33	72.69	3-stage cascode	[13] MWCL'09
		16.2	11.7	31.3	0.33	126.32		
		18	12	32.4	0.33	191.20		
90-nm CMOS	60	19.9	18.2	20.6	1.7575	55.60	4-way power combine	[2] ISSCC'10
65-nm CMOS	60.5	16.6	11	14.3	0.462	98.94	8-way power combine	[3] ISSCC'10
		18.1	11.5	15.5	0.462	139.75		
65-nm CMOS	60	16.8	13	18.9	0.83 (core)	59 (core)	4-way power combine	[4] ISSCC'10
		17.7	15.1	19.2	0.83 (core)	72.3 (core)		
65-nm CMOS	60	18.6	15	20.3	0.28 (w/o dc pads)	256 (w/o dc pads)	2-way power combine	[5] ISSCC'11
65-nm CMOS	60	18.3	16.9	18.8	0.19 (w/o dc pads)	355.8 (w/o dc pads)	4-way power combine	[6] CICC'13
90-nm CMOS	60	18.5	14.7	15.7	0.385 (core)	183.88(core)	3-stage CS+ 4-way power combine	[7] TMTT'13
90-nm CMOS	**63.2**	**22**	**17.8**	**15.0**	**0.49 (w/o pads)**	**323.4 (w/o pads)**	**Proposed Marchand Balun+ 4-Way Power Combine+ Proposed 90° Coupler**	**This Work**
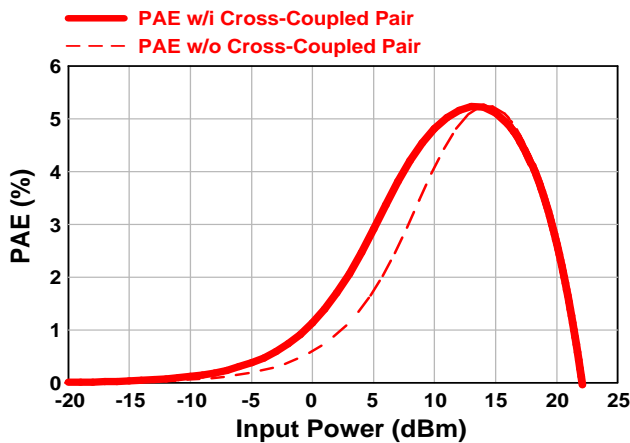
Fig. 8. Simulated PAE versus input power (after EM simulation) with and without the cross-coupled pair.

Fig. 8 illustrated the simulated PAE versus input power of the proposed PA with and without the cross-coupled pair. From this figure, it is observed that the PAE can be effectively improved because of the cross-coupled pair. Table I summarizes the recently published 60-GHz CMOS PAs along with this work. It is observed that the proposed PA can achieve the highest P_{SAT}, OP1dB, and power density (Saturated output power (P_{SAT})/Area).

IV. CONCLUSION

A 60-GHz power amplifier using 90-nm CMOS process has been proposed. Cross-coupled pairs are used to enhance the gain, output power, and PAE. In addition, the miniature Marchand balun and non-uniform-offset 90° coupler are proposed and introduced. By using these methods, the power performance of the PA can be effectively improved and superior to that of the recently reported 60-GHz CMOS PAs.

V. ACKNOWLEDGMENT

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