Double-Data Rate DDR Memory Review

Ahmed Shamil Mustafa, Mohammed Jabbar Mohammed, Muthana Najim Abdulleh

***Abstract*—Computer is one most important twenty-first century technology, the large volume of data and store it makes of old memories are not enough. In this paper we offer a historical overview of Double Data Rate (DDR) memory being play a key role in the development of computer with also who passed him in addition to the basics of their work and develop in the future.**

***Index Terms*—Double-Data Rate DDR, Synchronous Dynamic Random Access Memory (SDRAM)**

I. INTRODUCTION

In the twenty-first century with technology developments, the entry of the computer at all areas of scientific and social life. With the increased demand for computer and the large volume of data has become the task of manufacturing companies that meet the needs of the market. The old systems that were used become inadequate with modern software applications. So were developed memories to contain more information and increase the speed of the processor and also development the older generation of random access to DDR memory. That's one of the main functional computer its ability to store a lot of data in the unit that called memory. Specifically, RAM its random access memory; it is the function of saving the data that can be accessed at speed and directly. And for the ever growing system need for speed in addition to efficiency, understanding double data rate (DDR) memory is significant to organization developers [1]. The (DDR) double data rate that the development of the old model of (SDRAM) synchronous dynamic random access memory. The basis of the work of SDRAM it is waiting before responding meaning to say waits for clock signals before responding to control inputs. But DDR works both the falling with rising edges of the clock signal. So the DDR can transfer two times per clock cycle while SDRAM, one time per clock cycle [2]. With computer applications, DDR memory a larger scale used in other high speed, for example; graphic cards, which should require a lot of information to process in a short time to get and achieve the better graphics processing [1].

II. HISTORY AND DEVELOPMENT

When we want to talk about the history of DDR must know how works and what has been developed, so first we talking about technology SDRAM history because through this technique became DDR. The technology, synchronous dynamic random access memory (SDRAM) was discovered in the beginning 1990s to make the computer more powerful, in that time was used Traditional DRAM an asynchronous interface it means work independently of the processor. With the end of the nineties of the last century and the beginning of 2000s, specifically in 2000 became a priority for developers and manufacturers is to produce or something development new to increase the performance of the computer, DDR double data rate (also called DDR 1) is a new interface method was developed, this made data transfer on both the rising and falling edges of the clock signal it has the ability to transfer data twice faster than earlier versions, such as SDRAM, the had used lower clock rate (100-200MHz), less power (2.5v) and high speed(1600-3200 MB/s). With the continuing advancement of technology had made DDR 1 is not enough for it to be the issuance of a new generation DDR, It was followed DDR2 has appeared in 2003, an internal clock running at half the speed of DDR1 it means twice as fast as previous clock rate (200-533MHz), use less power (1.8 volts) and transfer rates up to (3200-6400 MB/s). In 2007 DDR3 became new generation of DDR, also speed was reduced to half of what it was the previous it is twice DDR2 speed clock rate (400-1,066MHz), use less power (1.5 volts) and transfer rates up to (6400-12800 MB/s).

Table 1: DDR Memory Characteristics

Type	Technology & generation	Rated clock (MHz)	Real clock (MHz)	Transfer rate (MB/s)
DDR - 200	DDR - SDRAM First generation	200	100	1600
DDR - 266		266	133	2100
DDR - 333		333	166	2700
DDR - 400		400	200	3200
DDR II - 400	DDR 2 - SDRAM Second generation	400	200	3200
DDR II - 533		533	266	4264
DDR II - 667		667	333	5336
DDR II - 800		800	400	6400
DDR III - 800	DDR 3 - SDRAM Third generation	800	400	6400
DDR III - 1066		1066	533	8528
DDR III - 1333		1333	666	10664
DDR III - 1600		1600	800	12800

They are three generation of DDR available [1].

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A. DDR1

Memory it is a first generation of DDR it became available in 2000 with rate clock 400 MHz, 8 byte (64-bit) of data bus and nowadays it is not produced in large quantities because of the presence of a generation produced after it

B. DDR2

Memory it is a second generation it became available in 2003 with data rate 400-800 MHz and 8 byte (64 bit) data bus, technology DDR physically incompatible with the old generation of memory DDR1.

C. DDR3

Memory it is a third generation it became available in 2007 with bandwidth (800 Mbps) and high speed, it is save a power compared to DDR2 memory it used 1.5 voltages.

III. UNDERLYING TECHNOLOGY OF DDR

A memory bank is a logical unit of storage in electronics, so it is a fundamental technology to work any memory, the consists of a bank of rows and columns, therefore number of bits in column or row equals to the memory bus width in bits. This technique is using in DDR memory and SDRAM memory. but the DDR to increase speed depended by work on an innovative way to double bandwidth without increasing the clock frequency it is exploit both the rising and falling edges of clock to transmit information also called double transition clocking. so DDR are using double transition clocking to transmit data without increasing the clock frequency and achieve data rate of 1.6 and 2.1 GB/s with frequency 100 MHz and 133 MHz, respectively [3]. DDR using many techniques to achieve high speed and this distinguish it from another memory; 2n-Prefetch Architecture, strobe-based data bus, different signaling technology,

A. 2n-Prefetch Architecture:

This techno mean it is the external data bus is half the width of an internal data bus, which is means fetch two word instead one word to read.

B. Strobe-based data bus:

The info capture rates are double clock frequency. The way it is usually that the region the location where the results are available (also known a data eye) is so small it is very difficult to satisfy setup and also hold right time to (the period of time that must pass to allow the signal to stabilize).

C. Signaling Technology:

The DDR technology using signaling technology, it means SSTL Stub Series Terminated Logic without depend low voltage LVTTL Transistor-to-Transistor Logic which used in another device [3].

IV. STRENGTHS AND WEAKNESSES OF DDR

The most significant advantage DDR is no other type of RAM combine large capacity and low cost, this make it best choice for customer. The row and column addresses are multiplexed over the same address pins, fewer pins are required to implement a given capacity of memory so it is makes efficient use of pins. the last advantages of DDR it is better one of using low power than an equivalent device [4-6]. In another side, with high capacity and low cost of DDR come additional complexity and latency. The complexity of the DDR interface requires that you always use a DDR controller to manage DDR refresh cycles, address multiplexing, and interface timing. Such a controller consumes FPGA logic elements that would normally be available for other logic. DDR suffers from a significant amount of access latency.

V. FUTURE ADVANCEMENTS

The need to increase the memory with the need to complete the tasks as soon as possible and less expensive, all this made, designers to speed development and to find alternatives. Is the new version of the developer standard memory that will replace DDR3 replaced, DDR 4 is designed to reliably manage at much higher speeds more and more than counterbalance the increased latency. In every way, DDR4 is actually superior to previous DDR3: the capable of being much faster, more effective, more scalable, and even more reliable. Regarding cost, much likes the transitions in order to DDR, DDR2, and also DDR3, DDR4 will end up progressively less expensive [7, 8]. When DDR4 is introduced, the initial 2133MHz and 2400MHz speeds will be accompanied by another increase in latency, just as each previous memory technology transition has been. These speeds are essentially the top of the ladder for DDR3, though; while DDR3 kits can be obtained at speeds as high as 3200MHz, ICs capable of performing at those levels are extremely rare. Meanwhile, DDR4 is expected to scale well beyond 3200MHz. What DDR4 offers is scalability for the future: individual DIMM densities start at 4GB and 8GB and are expected to scale to 16GB in 2015. Bandwidth is also capable of scaling up tremendously. 2666MHz DDR3 isn't especially common right now; it operates outside of JEDEC spec and requires carefully selected ICs, yet already situations exist that demonstrate a need for increased bandwidth beyond that speed. DDR4 comes out of the gate at 2400MHz, with 2666MHz, 2800MHz, and 3000MHz SKUs already planned. Finally, DDR4 operates at a nominal 1.2V and scales up to 1.35V, a reduction in operating power from DDR3's 1.5V standard and 1.65V mainstream high performance spec. Power efficiency has become increasingly important with each subsequent generation of CPU and GPU architecture from Intel, AMD, and NVIDIA, and DDR4 helps to enable that. DDR4 Physically In terms of the module, or DIMM it is a same DDR3 DIMM. Printed circuit board can be a slightly taller; the key notch is also in a different place. From the architectural new design DDR4 is designed to work at higher speeds, adds reliability not included in DDR3 and capacities with lower voltage, figure 3 shown maximum mainstream module size [7]. The main features in DDR4; bandwidth will be increased, density increased more reliability and lower power consumption.

VI. CONCLUSION

DDR SDRAM delivers faster performance at lower cost, which is necessary for industry-wide adoption. While the basic principle of DDR SDRAM is simple—transfer data on both the rising and falling edges of the system clock signal—the reality is that system designers had to solve several technical issues regarding signal integrity at the higher bus speeds. System designers were successful.

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REFERENCES

[1] J. Romo, "DDR Memories Comparison and overview," Beyond Bits, p. 70.
[2] J. A. Faue and J. Heightley, "System and method for supporting sequential burst counts in double data rate (DDR) synchronous dynamic random access memories (SDRAM)," ed: Google Patents, 2002.
[3] S.-H. Kim, W.-O. Lee, J.-H. Kim, S.-S. Lee, S.-Y. Hwang, C.-I. Kim, et al., "A low power and highly reliable 400Mbps mobile DDR SDRAM with on-chip distributed ECC," in Solid-State Circuits Conference, 2007. ASSCC'07. IEEE Asian, 2007, pp. 34-37.
[4] I. H. Veendrick, "Memories," in Nanometer CMOS ICs, ed: Springer, 2008, pp. 289-363.
[5] O. H.-D. RANDOM-ACCESS, "TESTING AND TESTABLE DESIGN OF HIGH-DENSITY RANDOM-ACCESS MEMORIES."
[6 Memory System Design. (2014). Available: http://www.altera.com
[7] S. Kyomin, N. Taesik, S. Indal, S. Yong, B. Wonil, K. Sanghee, et al., "A 1.2V 30nm 3.2Gb/s/pin 4Gb DDR4 SDRAM with dual-error detection and PVT-tolerant data-fetch scheme," in Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International, 2012, pp. 38-40.
[8] P. Nam, D. Dreps, R. Mandrekar, and N. Nanju, "Driver design for DDR4 memory subsystems," in Electrical Performance of Electronic Packaging and Systems (EPEPS), 2010 IEEE 19th Conference on, 2010, pp. 297-300.

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