Comparative Study on Low Power Barrel Shifter/Rotator at 45nm Technology

Jyoti Sankar Sahoo, Nirmal Kumar Rout

Abstract*-- As technology advances in the field of VLSI; the circuits are upgraded to less power consuming and of high speed. In modern digital signal processing (DSP) and graphics application the shifter is an important module. A Barrel shifter/rotator can be implemented exclusively for shifting and rotating operations individually or both at the same time and can be implemented by 2:1, 4:1, 8:1 etc. multiplexers units. Barrel shifter/rotator implemented using multiplexer unit can use it repeatedly thus reduce the amount of power consumption. In this paper initially the Barrel shifter/rotator circuit using multiplexer is implemented using Complementary Metal Oxide Semiconductor (CMOS) logic then the circuit is implemented by different low power techniques. Finally various designs are compared in terms of power and delay. All the designs are implemented in Cadence Virtuoso Tool at 45nm technology for its validation.

***Index Terms*—Barrel shifter, Pass transistor logic, LECTOR technique, Double gate MOSFET, Diode Free Adiabatic Logic, Low power.**

I. INTRODUCTION

As the technology is scaling down towards the deep submicron level, the digital circuits become complex. So this indirectly affect the power consumption and the speed of the circuit. A barrel shifter is a combinational logic circuit which shift a data by any given number of bits, in a single operation. Many applications such as in CPU, variable length coding, word packing/unpacking, bit indexing, address generation etc required Barrel shifter/rotator circuit exclusively for the shifting and rotating operations [1]. Barrel shifter/rotator circuit is implemented in both general purpose processor and digital signal processor [2]. The circuit is designed with multiplexer unit for its better performance. Various techniques are adopted to implement Barrel shifter/rotator circuit. But according to the recent trends the circuit needs to be implemented with low power techniques which reduce the overall power consumption without affecting the processing speed. Initially the circuit is implemented with complementary metal oxide semiconductor (CMOS) logic but in that design the power consumption was severely high. So in this paper four different low power design techniques such as pass transistor logic technique, LECTOR technique[3], Double gate metal oxide semiconductor field effect transistor (MOSFET) technique[4] and Double gate MOSFET with Diode Free Adiabatic Logic(DFAL) were adopted to implement a Barrel shifter/rotator circuit.

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Mr. Jyoti Sankar Sahoo, Electronics and Communication Engineering, KIIT University, Bhubaneswar, Odisha, India.

Dr. Nirmal Kumar Rout, Assoc. Prof. Electronics and Communication Engineering, KIIT University, Bhubaneswar, Odisha, India.

All the designs are compared with respect to power and delay with different supply voltages and the results are tabulated in the concerned section. The proposed Double gate MOSFET with DFAL technique is efficiently reduce the power consumption in the given circuit. The LECTOR technique is effective in delay reduction. The techniques are explained in detail in the following sections. The paper is organized with six sections. The second section includes brief description on Barrel shifter/rotator circuit and it's working principle. The third section describes different low power methods to implement the Barrel shifter. The fourth section introduced the proposed low power design of Barrel shifter/rotator. Fifth section shows the simulation results of the different low power methods and compare the results in terms of power and delay. The last section is the conclusion section which describes the effective design technique in terms of power and delay.

II. BARREL SHIFTER/ROTATOR CIRCUIT

A. Shifters

Barrel shifter is a combinational circuit which shifts data with a precise number of bits within a single clock cycle . It has N number of inputs and N number of outputs and a set of control inputs. In this paper the Barrel shifter is implemented using multiplexer unit. And this design connects output of one multiplexer block to the input of the next multiplexer block in a way that depends on the shift distance. The number of multiplexer units needed for the implementation of N bit Barrel shifter is calculated as $N \log 2(N)$, [5,6] where N represents the number of input bits. The shifting operation is tabulated below in Table 1.

TABLE I. SHIFTING OPERATION OF 8 BIT BARREL SHIFTER

c2	c1	c0	y 7	y6	y5	y4	y3	y2	y1	y0
L	L	L	a7	a6	a5	a4	a3	a2	a1	a0
L	L	H	a0	a7	a6	a5	a4	a3	a2	a1
L	H	L	a1	a0	a7	a6	a5	a4	a3	a2
L	H	H	a2	a1	a0	a7	a6	a5	a4	a3
H	L	L	a3	a2	a1	a0	a7	a6	a5	a4
H	L	H	a4	a3	a2	a1	a0	a7	a6	a5
H	H	L	a5	a4	a3	a2	a1	a0	a7	a6
H	H	H	a6	a5	a4	a3	a2	a1	a0	a7

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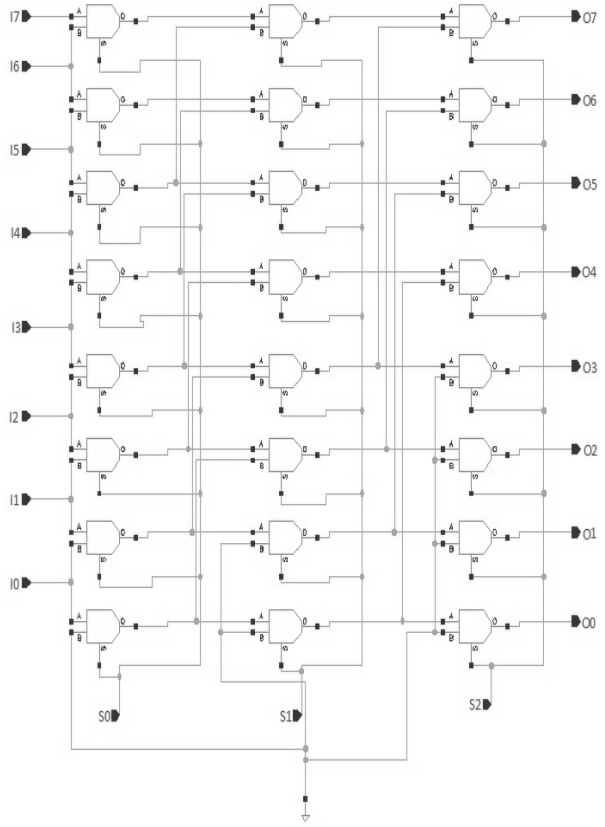

Fig. 1. Schematic of 8- bit Barrel shifter

From the above table "**c**" denotes the select line set or the control line set, "**a**" is the input vector of size 8-bit and "**y**" is the output vector of size 8-bit. "**L**" is the low state and "**H**" is the high state. In this paper the Barrel shifter circuit is implemented with multiplexer units. The design of Barrel shifter is shown in Fig. 1. The multiplexer units are initially designed with CMOS logic and later implemented with different low power designs that are described in section III.

B. Rotator

The 8-bit rotator circuit uses three stages with 4-bit, 2-bit, and 1-bit rotates. In a rotator circuit, as every input bits are routed to the output, hence there is no need for interconnect lines carrying zeros. But the interconnect lines are inserted to enable routing of the 2^k low order data bits to the 2^k high order multiplexors in the stage controlled by b_k. The design of right rotator is shown in Fig.2. The 8-bit right rotator as shown in Fig.2 is divided into three levels. The first level provide four bit right rotate and this level is controlled by control input "b0". The second level provide two bit right rotate and is controlled by the control input "b1". The last level provide one bit right shift and can be controlled by the control input "b2".

C. Multiplexer based Right Shifter and Rotator

The logical right shifter can be extended to right shifter and rotator by adding extra multiplexer units. The design is shown in figure 3. Here also has three levels of operation. The first level shows four bit right shift/rotate, the second level shows two bit right shift/rotate and the last level shows one bit of shift/rotate. Initially, a single multiplexor selects between '0' for logical right shifting and A_{n-1} for arithmetic right shifting to produce *S*. The stage inhibited by b_k, 2^k multiplexors select between *S* for shifting and 2^k lower bits of data for rotating.

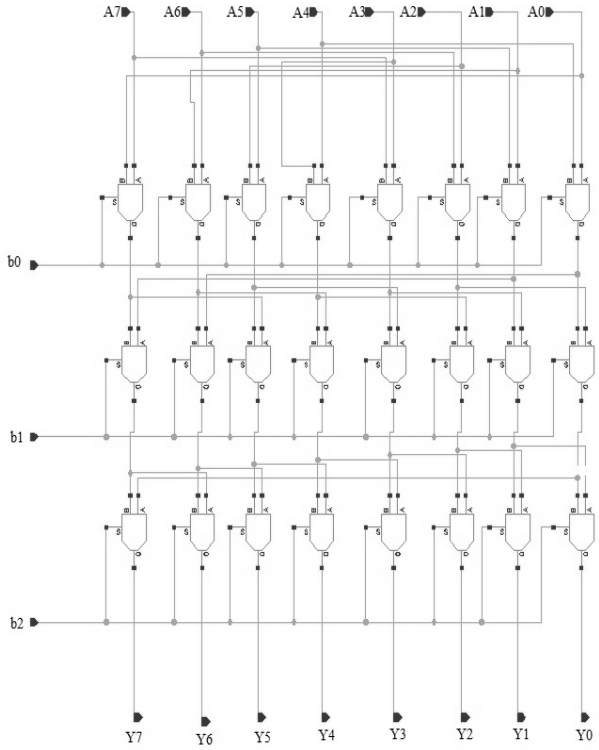

Fig. 2. Schematic of 8 bit-Right Rotator

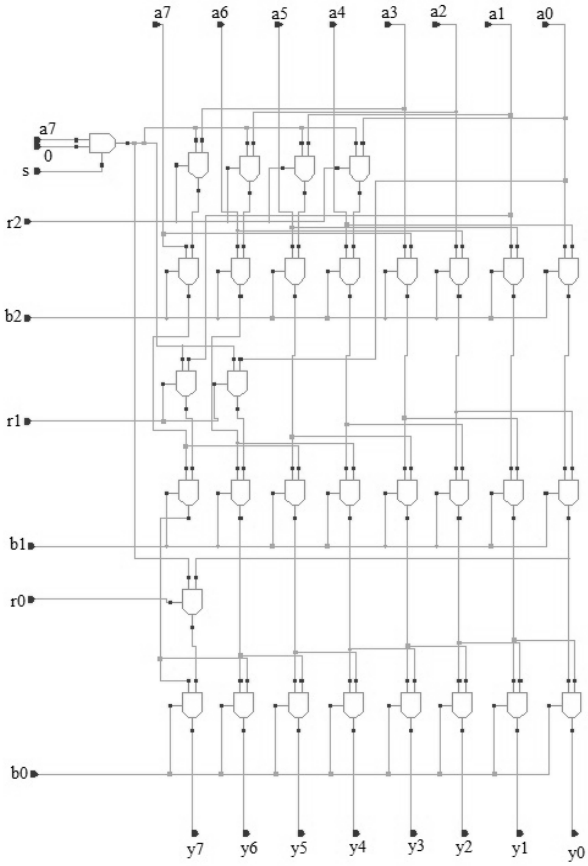

Fig. 3. Schematic of 8-bit Right shifter/rotator

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III. LOW POWER TECHNIQUES FOR IMPLEMENTING THE BARREL SHIFTER/ROTATOR CIRCUIT

The Barrel shifter/rotator circuit is implemented by multiplexer units. These multiplexer units are designed with the following listed low power techniques.

A. Pass Transistor Logic

In pass transistor logic the primary inputs are allowed to drive not only the gate terminal but also the source/drain terminal of the MOSFET unlike the complementary MOSFET, in which the primary inputs are only to drive the gate terminal [7]. So the number of transistors used are reduced, hence reducing area as well as delay. The multiplexer using pass transistor logic is shown in Fig. 4.

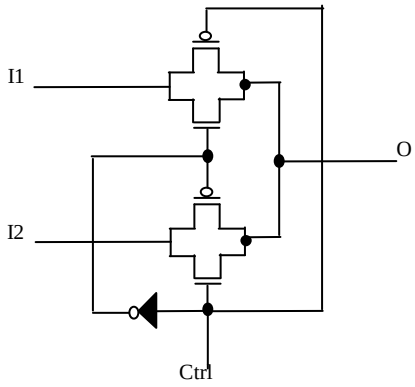

Fig. 4. 2:1 Multiplexer using pass transistor logic

B. LECTOR Technique

The LECTOR technique is basically concerned with the leakage power reduction in a circuit by introducing the stacking transistors between the supply and the ground [8]. This technique includes two Leakage control transistors (LCTs) in a CMOS gate between the pull up and pull down networks and the gate terminal of one transistor is inhibited by the source terminal of other. With the above arrangement one of the LCT is operated with its cut-off region. The technique is shown in Figure 5. In this paper the multiplexer units are implemented with LECTOR technique exhibit very less delay compare to the other low power techniques. The calculation results of delay and power is described in section V.

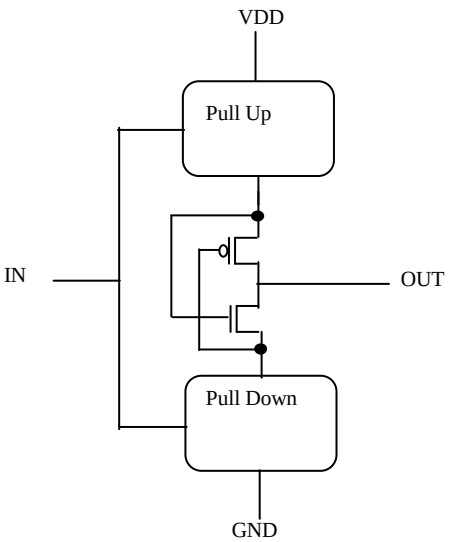

Fig. 5. LECTOR Technique

C. DFAL Technique

In this Diode free adiabatic logic (DFAL) approach the circuit function is separated into two phases such as evaluation phase and hold phase [9] according to the supply clock signal phases. In the evaluation phase V swings up and V_{bar} swings down and during the hold phase the reverse happens. During evaluation phase when output is *Low* and pull up network i.e. PMOS network turned ON, the load capacitance C_L is charged which produce *High* state as output. And when output is *High* and pull down network i.e. NMOS network turned ON the load capacitor discharges through the NMOS transistors which results the output logic *Low* state. Similarly in the hold phase when the output is *Low* and pull down network is turned ON then no transitions occur at the output and when the state of the output is *High* and the PMOS is turned ON the C_L is discharging [10]. Due to the switching the dynamic switching is reduced thus reducing the energy dissipation. The DFAL logic is shown in Fig. 6. The DFAL technique is very efficient for the average power reduction of the total circuit. Here the multiplexer units are designed with this technique and then with these multiplexer unit the Barrel shifter/rotator circuit are implemented.

D. Double Gate MOSFET

Double gate MOSFET structure is emerging as the most prominent technology for low power circuit designs. The double-gate MOSFET has a channel of scaled width and to manage that channel, gates are provided to both the sides [4]. The two types of gates namely the Front gate and Back gate in this device can be independently driven for the purpose of reduction in power consumption and improve the performance of the device [11]. Double gate MOSFET devices are otherwise known as scalable silicon transistors because of its tremendous control over the short-channel effects in the double-gate structure [12, 13].

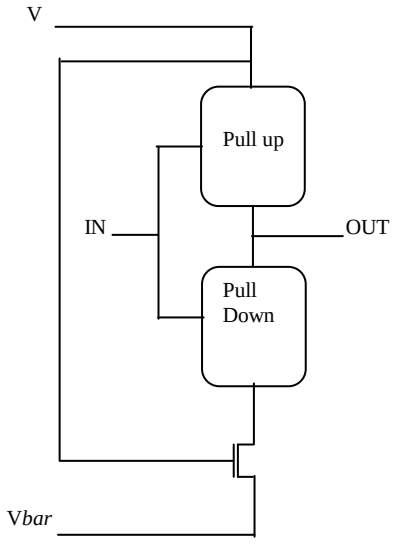

Fig. 6. DFAL Logic

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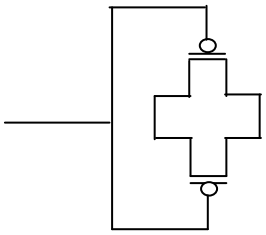
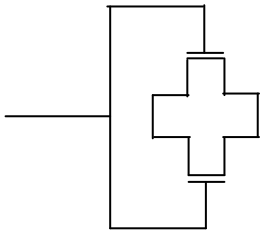


(a) P-type



(b) N-type

Fig. 7. Types of Double gate MOSFET

Fig. 7 shows the diagram of symmetric tied P-type and N-type double gate MOSFET. The double gate MOSFET can be asymmetric type and can be individual (i.e. the gates are connected to different voltage supplies). In this paper the multiplexer units are also implemented with this double gate MOSFET technique and thus the Barrel shifter/rotator circuit too.

IV. PROPOSED TECHNIQUE

In this paper a new technique is proposed which is the combination of double gate MOSFET and DFAL technique. This new technique found to be efficient in both delay and power reduction. The logic of the new technique is shown in Fig.8.

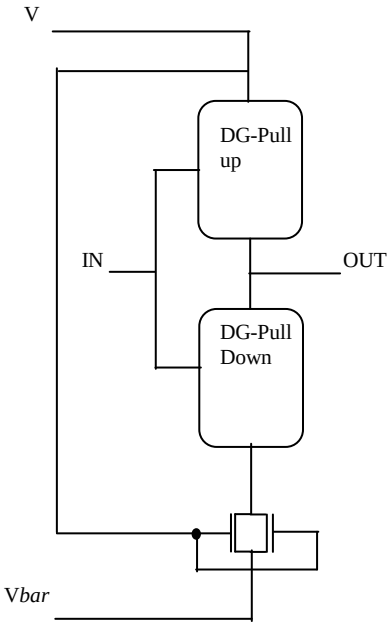


Fig. 8. Double gate-DFAL Logic

In this proposed technique the inner circuit i.e. the pull up and pull down network is implemented with double gate MOSFET. The N-type footer transistor used in the DFAL logic is also converted to N-type double gate MOSFET transistor the source of which is connected to the V_{bar} input. The schematic of 2:1 multiplexer unit implemented with this new technique is shown in Fig.9.

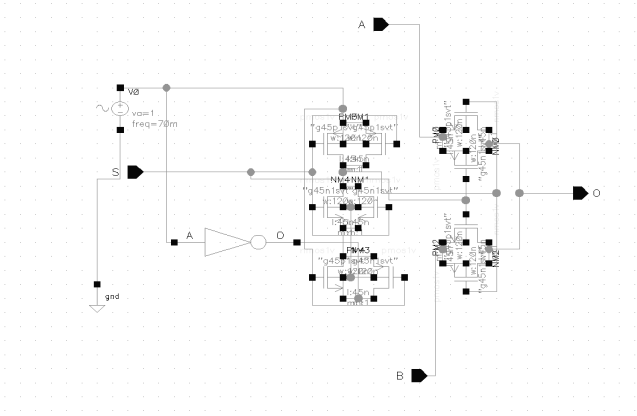


Fig. 9. 2:1 Multiplexer using the proposed technique

A. Operation

Suppose select line is high. At that time, DFAL inverter output becomes low and select line directly gets connected to NMOS, as a result of this PMOS and NMOS transistor gets ON. Input B comes to output. Suppose select line is low, at that time DFAL inverter output becomes high and select line directly connected to PMOS, so both PMOS and NMOS transistor turns on, and A input comes to output. The V and Vbar inputs are supplied with sine wave of 180º phase and 100M Hz frequency. The output waveform of the multiplexer unit is shown in Fig. 10. With this method the average power as well as the delay of the multiplexer unit reduces to an appreciable amount. The comparison of average power and delay of 2:1 multiplexer unit with different power reduction techniques is shown in Table.2.

TABLE. II. COMPARISON OF AVERAGE POWER AND DELAY OF 2:1 MULTIPLEXER

Multiplexer Designs	Average Power (nW)	Delay (nS)
CMOS Logic	79.24	30.2
Pass Transistor Logic	102.20	30.25
LECTOR Technique	39.37	29.64
DFAL Technique	36.73	20.11
Double gate MOSFET Logic	34.08	27.19
Proposed Technique	**31.73**	**20.04**

From the above table it is quite clear that the proposed technique is effective in delay and average power reduction of the multiplexer circuit. The output waveform of the 2:1 multiplexer unit using the proposed technique is shown in Fig. 10.

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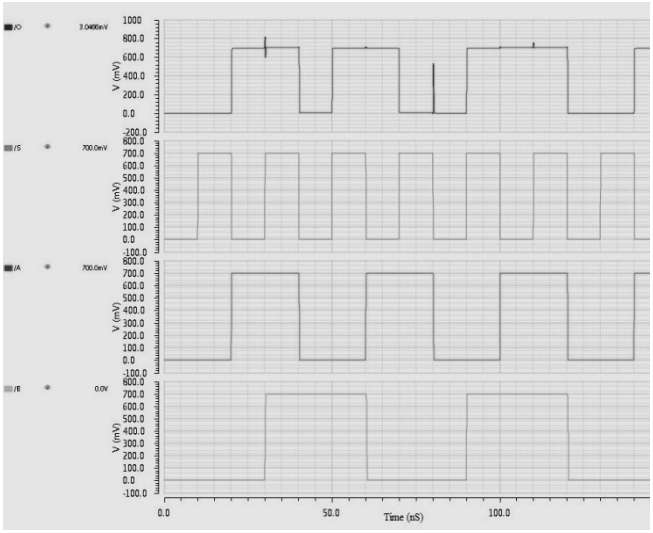

Fig. 10. Input- Output waveform of 2:1 multiplexer using the proposed technique

The 2:1 multiplexer units designed with this technique are later implemented in the Barrel shifter/rotator circuit as shown in Fig.1, Fig.2, Fig.3. The power and delay of all the implemented designs are compared in section V with different supply voltages. All the designs of shifter/rotator circuits are implemented in Cadence Virtuoso Tool at 45nm technology.

V. SIMULATION RESULTS AND DISCUSSION

The simulation of Barrel shifter/rotator unit have been carried out at 45nm technology with different supply voltages and comparison of different techniques have been discussed in terms of average power and circuit delay.

A. Simulation of Shifter circuit

The shifter circuit shown in Fig.1 has been implemented by the multiplexer units. Those multiplexer units are implemented with different low power techniques as described in section III. The output waveform of 8 bit Barrel shifter is shown in Fig. 11. The average power and delay of the different Barrel shifter designs are tabulated in Table. III.

TABLE. III. POWER AND DELAY OF DIFFERENT LOW POWER DESIGN IMPLEMENTATION OF SHIFTER

8 bit Shifter Designs	Average Power (nW)	Delay (nS)
CMOS Logic	1926.00	89.87
Pass Transistor Logic	781.20	40.63
LECTOR Technique	913.20	31.05
DFAL Technique	1023.56	37.12
Double gate MOSFET Logic	564.34	40.12
Proposed Technique	**421.9**	**30.36**

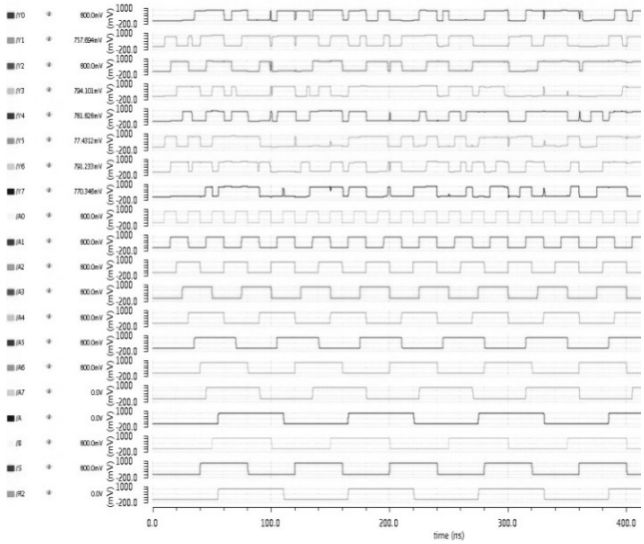

Fig. 11. Input-Output waveform of 8 bit Barrel shifter

From Table. III it can be well observed that with the proposed technique the average power of the Barrel shifter circuit reduced to a large extent as compare to the previous techniques. Also the circuit delay decreased to an appreciable limit as compare to the stated techniques. The data tabulated in Table.III are collected by taking the supply voltage of 0.7V. The average power and delay comparison chart is shown in Fig. 12.

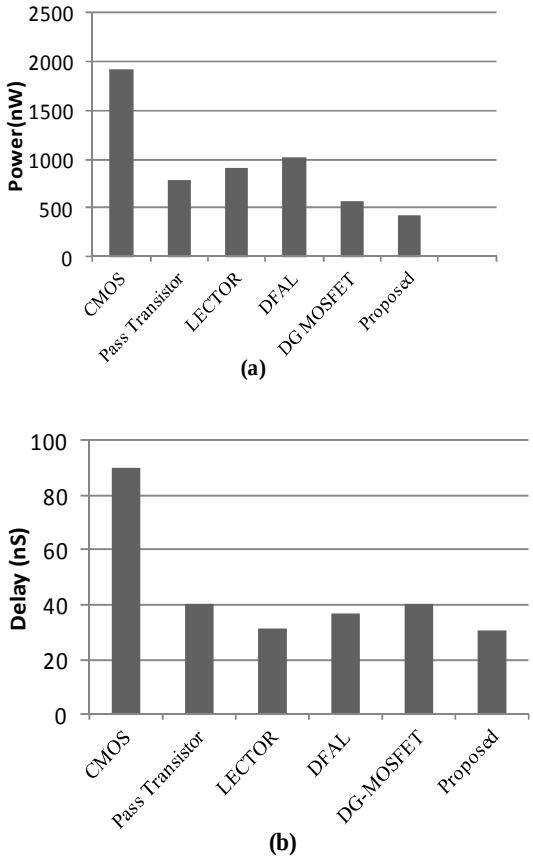

Fig. 12. Average power and Delay comparison chart

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B. Simulation of Rotator circuit

The 8 bit right rotator circuit as shown in Fig.2 has been implemented with the 2:1 multiplexer units with the low power techniques which described in section III. The multiplexer units are also implemented with the proposed technique and compared with the previous techniques with respect to average power and delay. The output waveform of the rotator is shown in Fig. 13. and the comparison table of average power and circuit delay is shown in Table. IV. The comparison chart of average power and delay according to the Table. IV is shown in Fig.14.

TABLE. IV. COMPARISON OF POWER AND DELAY OF 8 BIT ROTATOR CIRCUIT.

8 bit Rotator Designs	Average Power (nW)	Delay (nS)
CMOS Logic	3021	129.4
Pass Transistor Logic	1526	95.5
LECTOR Technique	1506	121.7
DFAL Technique	1096	57.28
Double gate MOSFET Logic	1130	63.51
Proposed Technique	**1006**	**30.28**

According to Table. IV the 8 bit rotator circuit performed well with the proposed design as the average power dissipation and circuit delay reduces to an appreciably mark.

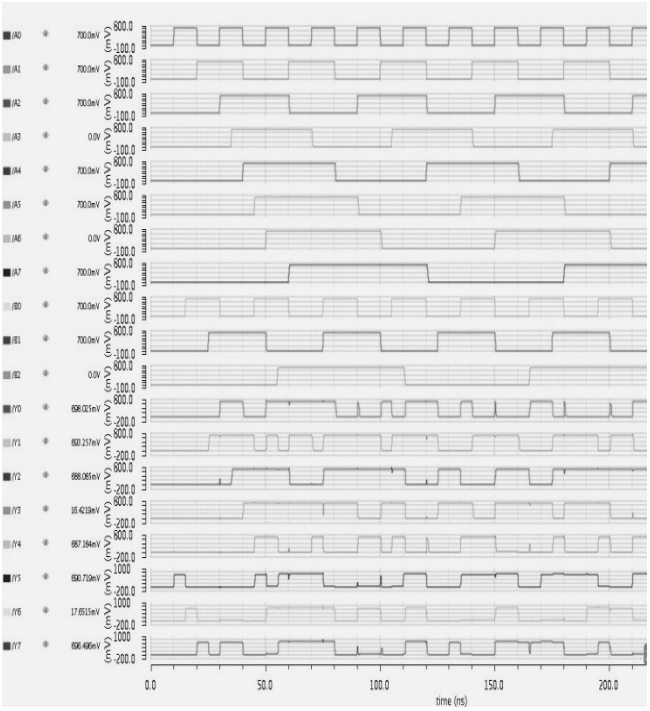

Fig. 13. Input-Output waveform of 8 bit Rotator circuit

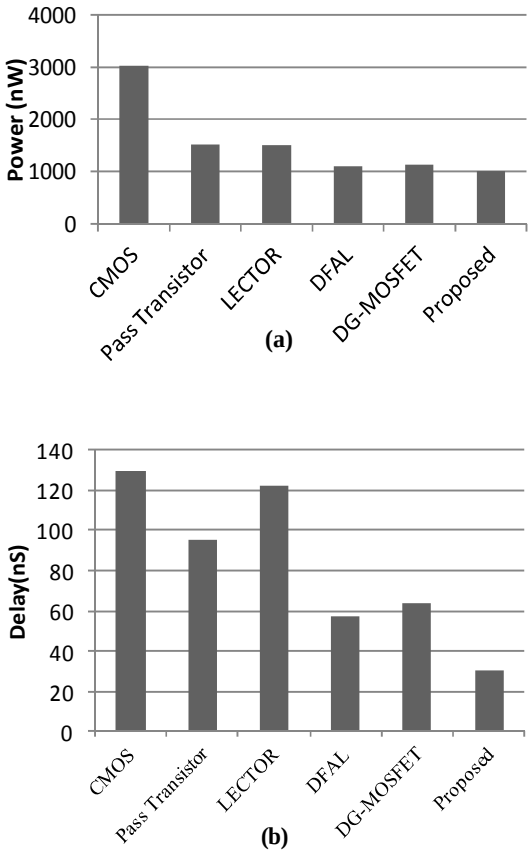

Fig. 14. Comparison chart of average power and circuit delay of 8 bit Rotator circuit

C. Simulation of Shifter/ Rotator Circuit

Figure. 3 shows the 8 bit Barrel shifter and rotator circuit. The circuit is implemented by 2:1 multiplexer units with the power reduction techniques described in section III and also with the proposed technique at different supply voltages such as 0.8V, 0.7V and 0.6V. The input and output waveform is shown in Fig. 17 and the average power and circuit delay is tabulated in Table. V. The designs are implemented with Cadence Virtuoso Tool at 45nm technology. Fig. 18, Fig. 19, Fig. 20 shows the comparison chart of power and delay of shifter/rotator circuit at 0.8V, 0.7V and 0.6V supply voltage.

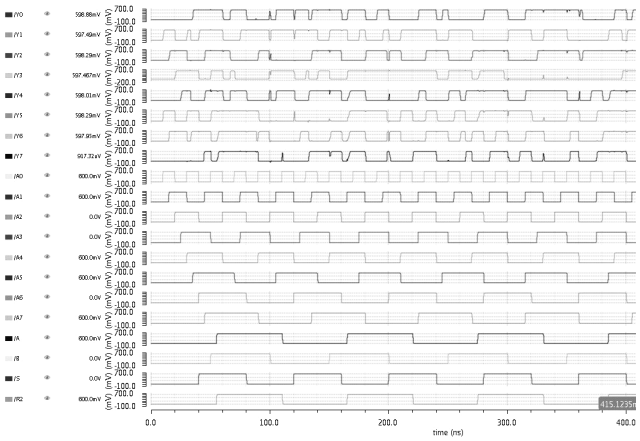

Fig. 15. Input-Output waveform of Barrel shifter/rotator circuit

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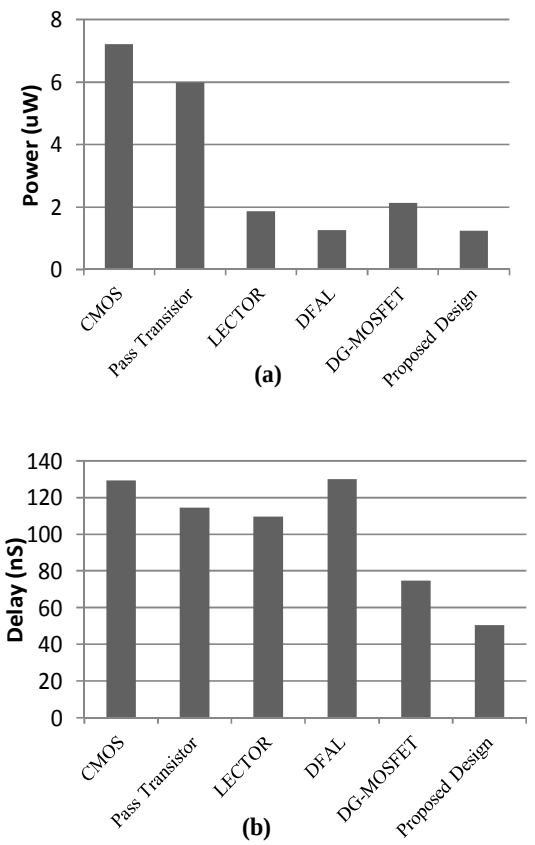

Fig. 16. Comparison chart of power and delay of shifter/rotator circuit at 0.8 V supply.

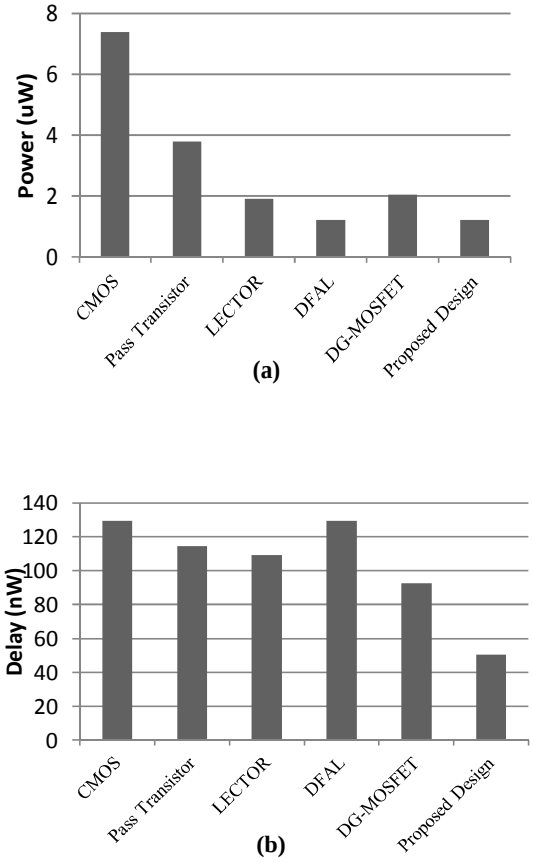

Fig. 17. Comparison chart of power and delay of shifter/rotator circuit at 0.7V supply

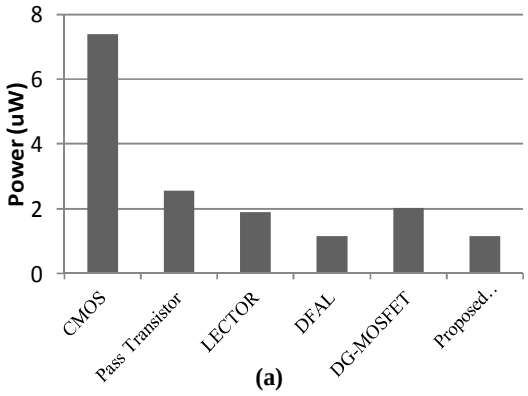

TABLE.V COMPARISON OF AVERAGE POWER AND DELAY OF 8 BIT BARREL SHIFTER/ROTATOR CIRCUIT

Shifter/Rotator Design	Supply Voltage (0.8V)		Supply Voltage (0.7V)		Supply Voltage (0.6V)	
	Power(uW)	Delay(nS)	Power(uW)	Delay(nS)	Power(uW)	Delay(nS)
CMOS	7.228	129.4	7.390	129.4	7.397	129.3
Pass Transistor	5.984	114.6	3.778	114.5	2.547	114.1
LECTOR	1.863	109.4	1.911	109.3	1.885	109.2
DFAL	1.273	129.9	1.202	129.4	1.154	129.7
DG-MOSFET	2.135	74.68	2.043	92.52	2.014	104.2
Proposed Design	**1.245**	**50.42**	**1.201**	**50.45**	**1.147**	**49.47**

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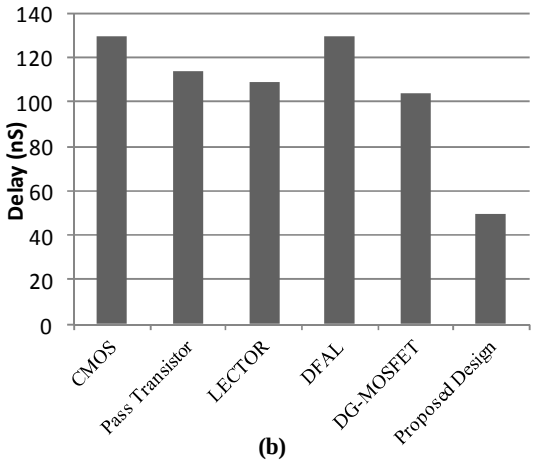

Fig. 18. Comparison chart of average power and delay of shifter/rotator at 0.6V supply

VI. CONCLUSION

As the technology scales down the sub threshold leakage current dissipation of the total circuit increases which also affect the circuit performance. So the circuit design implementation need to be upgraded so as to manage the power and delay issues. In this paper various low power design techniques have been described and Barrel shifter/rotator circuits were implemented with these techniques. We have presented an efficient design methodology for reducing the power dissipation in VLSI design. The proposed technique of this paper is much more effective in average power and delay reduction of the concerned circuit as compared to the previously described techniques. The designs were implemented with Cadence Virtuoso Tool at 45nm technology for its validation.

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Jyoti Sankar Sahoo, M.Tech in VLSI Design and Embedded System, KIIT University, Bhubaneswar. He received his Bachelor of Technology(B.Tech) degree from REC, Bhubaneswar in the year 2012. His interested research area are low power VLSI circuit design and memory design etc.

Dr. Nirmal Kumar Rout, Working as an Associate Professor in the Department of Electronics and Communication Engineering, KIIT University. His area of interest are Digital Signal Processing, Low power VLSI circuit design, memory design etc.

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